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Student Training Manual for

**CYBER 170 MODEL 720/730
CENTRAL PROCESSOR**

VOLUME 1

An Individualized Course

[illegible]

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Printed in the United States of America

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INTRODUCTION

This course is an individualized, self-study course designed to provide you with an understanding of the CYBER 170 Models 720/730 CPU. You will systematically proceed through 12 modules in such a way as to cover the location, identification, and description of the logic associated with the control signals and data flow for each section of the CYBER 170 Models 720/730 CPU. Module 12 is a laboratory module which provides hands-on troubleshooting of the entire CPU.

The diagrams and theory of operation description used in this course relate to the CYBER 170 Models 720/730 CPU, but the CYBER 170 Models 720, 173 CPUs may be related to very closely by the use of the appropriate diagrams for the Models 172 and 173.

Since this course is individualized, you will proceed through each learning activity at your own pace and dependent upon your comprehension of the material. You will be assigned reference reading and text reading, often followed by exercises designed to test your comprehension of the assigned material. You will also be given a post test at the completion of each module which must be passed prior to proceeding to the next module. You may elect to pretest on a newly assigned module which may allow you to skip activities that you may already comprehend.

If this is your first experience with PLATO assisted learning (PAL) you may want to read through appendix A, Introduction to PLATO Assisted Learning before you actually sign on to the terminal. That appendix explains to you the basic philosophy and organization of the self-study courses. It also explains the correct procedure to sign on to the PLATO terminal.

You may now begin the course by reading the next page and following the instructions there.

MODULE 1

INTRODUCTION TO CYBER 170

MODELS 720, 730 CPU

During this module you are introduced to the course and are provided a review of the CPUs operation at a simplified block diagram level. You also will learn more about the CPU at a more detailed block diagram level.

PRETEST

To start this module, sign on to the PLATO terminal and read the objectives. If you feel that you might be able to meet some of the objectives, take the module test. After evaluating the results of your test, PLM will assign the learning activities that relate to the objectives you did not meet. If you do not wish to take the test first ask for an assignment.

LEARNING ACTIVITIES

In the Assigned column, put a check mark by each activity assigned to you by PLM. Then proceed through your assigned activities. Check off each activity as you complete it. You may choose to do all the activities or do some activities more than once.

<u>Assigned</u>	<u>Completed</u>	<u>Activity</u>	<u>Description</u>	<u>Page</u>
_____	_____	1-A	Text Reading: Course Introduction. This learning activity introduces the CYBER 170 Models 720, 730 CPU Maintenance course.	1-3
_____	_____	1-B	Text Reading: CPU Functions. This learning activity covers the concepts of the CPU operation.	1-5
_____	_____	1-C	Audio/Microfiche: Simplified Block Diagram. This learning activity covers the function and purpose of the various registers and sections of the serial CPU.	1-8

CYBER 170 Model 720/730 CPU
Module 1

<u>Assigned</u>	<u>Completed</u>	<u>Activity</u>	<u>Description</u>	<u>Page</u>
_____	_____	1-D	Exercise: Review of CPU Block Diagram. This learning activity reinforces what you learned about CPU functions.	1-10
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_____	_____	1-G	Audio/Microfiche: Data Flow. This learning activity covers basic instruction execution and data flow for central memory accesses.	1-21
_____	_____	1-H	Exercise: Review of Data Flow. This learning activity reinforces what you learned about the serial processor operations and data flow.	1-23
_____	_____	1-I	Text Reading: CPU Characteristics and Interfaces. This learning activity covers the CYBER 170 Model 720, 730 CPU characteristics and the CMC to ECS/ESM interfaces.	1-25
_____	_____	1-J	Text Reading: Detailed Block Diagram. This learning activity covers the CYBER 170 Models 720, 730 CPU detailed block diagram.	1-29
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LEARNING ACTIVITY 1-A. TEXT READING: COURSE INTRODUCTION

This learning activity introduces the CYBER CPU 170 Models 720 and 730 Maintenance course.

OBJECTIVE

- You will be able to identify the training procedures and the required documentation necessary to complete the CYBER 170 Model 720, 730 CPU Maintenance course.

Before you get started, you should ensure that you have all the manuals required to complete this course. Following is a list of the manuals you will need.

<u>Title</u>	<u>Publication Number</u>
CDC CYBER 170 Computer Systems Models 720, 730, 740, 750, 760 Hardware Reference Manual	60456100
CDC CYBER 170 Models 720, 730 Central Processing Unit Hardware Maintenance Manual (Logic Diagrams & Theory of Operations)	60456170
CDC CYBER 170 Models 720, 730 Central Memory Control Hardware Maintenance Manual (Diagrams and Theory of Operation)	60456180
6000/CYBER 70/CYBER 170 SMM Reference Manual	60160600
6000/CYBER 70/CYBER 170 SMM Supplement	60409500
6000/CYBER 70/CYBER 170 Instant SMM	60299500

If you do not have all the manuals listed above, contact your course administrator for assistance in obtaining them.

This course is an individualized, computer managed course which teaches you how the CYBER 170, Models 720, 730 CPU operates and how to maintain the CPU section of the mainframe.

All testing is performed on the PLATO system. As you complete your studies of the lessons in each module you should sign-on to the PLATO system and take the test for the module. The tests are written to evaluate your knowledge and ability as stated in the objectives of

CYBER 170 Model 720/730 CPU
Learning Activity 1-A

this course. After completion of your test, PLATO will evaluate the results and give you a study assignment which teaches any objective you did not master. If you master all the objectives, you will be able to progress to the next module in the course.

If, while you are signed-on to PLATO, you wish to make a comment on anything in this course you may do so. To make a comment, press the SHIFT key and the TERM key on the keyboard simultaneously. On the bottom of your screen you will be asked: "What term?" At this point type the word "comment". You will then be able to type in your comment. When you are through inputting your comment, press SHIFT-NEXT and your note will be stored and automatically forwarded to Engineering Services Education personnel for their review.

If your problem is of an immediate nature, it is recommended that you contact your technical advisor or course administrator for assistance. The comment feature will not give you immediate results, but you can be assured that all comments are read and noted by ESE. If your comment warrants a change in the course, it will be done by an ESE course developer as soon as possible. Your comments are solicited and provide a valuable means of keeping ESE courses current.

To complete this course you will need to have a microfiche viewer and an audiotape cassette player. Again, if you do not have these, contact your course administrator.

At this time you are ready to begin the course. If you have already taken your module 1 pretest, you should proceed with the assignment given to you. If you have not taken the module 1 test, you may wish to do so at this time to find out what areas you need to study.

LEARNING ACTIVITY 1-B. TEXT READING: CPU FUNCTIONS

The CPU is the last portion of the CYBER mainframe to be studied. This learning activity covers the concepts of the CPU's operations.

OBJECTIVE

- You will be able to state the functions the CPU serves within a CYBER system.

As you recall, the CPU is the section of the mainframe that performs the principal arithmetic operations for the system. In order to perform the arithmetic operations as fast as possible, the CPU section has been relieved of all I/O operations. The PPU's have the I/O responsibility. The CPU can only access CM through CMC. The CPU's programs must be stored in CM by the PPU's; the CPU can then execute the program. When the program is completed, the results are in CM; the PPS section will be responsible to output the information.

In addition to being free from I/O responsibility, the CPU has another feature that allows it to execute instructions faster. This feature is called the operating register (refer to figure 1-1). The CPU has a series of operating registers that are used to temporarily hold operands. When the CPU executes an arithmetic instruction, it used the operating registers for the source operands; it also used the operating register as a result register to hold the answer derived by the instruction.

Accessing the operating registers is much faster than accessing CM for each operand. Therefore, the CPU programs are written to perform as many operations as possible using the operating registers. Of course, the program eventually will have to get new operands from CM and store results in CM. Until that need arises, however, the CPU computes results at a very high rate. When the new operands are read from memory, the same type of operation can take place again. This description of the CPU's operating registers is brief, but you will learn more about them later in this module.

The CPU can perform arithmetic operations in a fixed point (whole integer) format and also in the floating point (scientific notation) format. As you will see in future activities, the floating point format gives the CPU an extremely large range of number values to work with.

Another function of the CPU is to command CMC and CM to transfer data to or from the ECS subsystem. When the CPU program needs to access ECS, it stops the CPU and commands CMC to perform the transfer operation at the addresses specified by the CPU.

CYBER 170 Model 720/730 CPU
Learning Activity 1-B

There are two types of CPUs in the CYBER product line: the serial processor and the parallel processor.

The serial processor is sometimes called a sequential type processor. Basically, a serial processor is one that can execute one instruction at a time. As soon as one operation is completed, it starts the next one. Each instruction tells the CPU hardware what to do and which operating registers to use during the instruction sequence defined by the control section of the CPU. The CYBER 72 and CYBER 73 models, the CYBER 171, 172, 173, and 174 models, and also the CYBER 170, models 720 and 730 have the serial processor CPU.

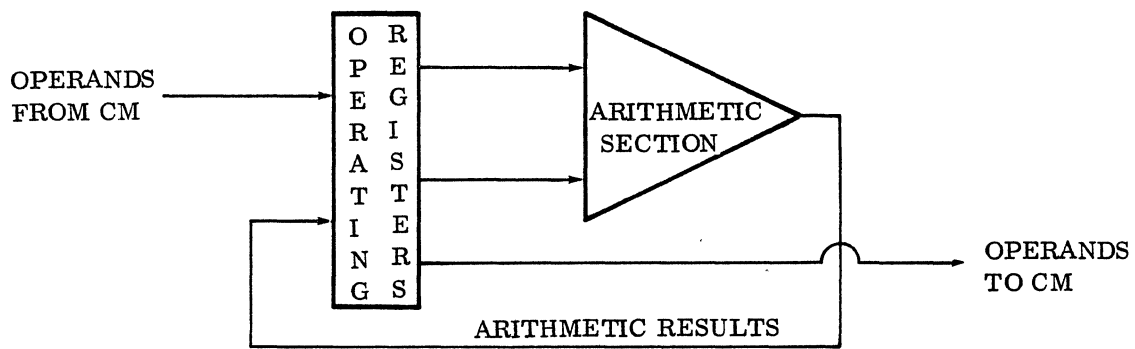


Figure 1-1. Simplified CYBER CPU Diagram

The parallel processor is sometimes called a concurrent processor. This type of processor has the ability to have more than one instruction in execution at a time. The hardware in the parallel processor that allows this action to happen consists of the functional units. A functional unit is a specialized piece of hardware that can perform only one type of arithmetic function. Each functional unit operates independently of the others. If the CPU reads an instruction to multiply two numbers, the control section will command the multiply unit to perform the operation and also tell it which operating registers to use. Immediately after the functional unit starts, control looks at the next instruction. If it is not a multiply and/or does not require the same operating registers, the control section will tell another functional unit to start. It may be an add, subtract, divide, or Boolean operation.

You can see that this concept can greatly increase the throughput of a parallel CPU. The CYBER 74, CYBER 175, CYBER 176 Models, and also the CYBER 170 Models 740, 750, and 760 models have the parallel CPU.

CYBER 170 Model 720/730 CPU
Learning Activity 1-B

During this course you will be learning the hardware operation and maintenance of the CYBER 170, Models 720 and 730 CPU.

This concludes the activity on CPU concepts. In the remaining activities in this module you will learn more about the items covered in this lesson.

LEARNING ACTIVITY 1-C. AUDIO/MICROFICHE: SIMPLIFIED BLOCK DIAGRAM

During this activity you learn the function and purpose of the various registers and sections of the serial type of central processor.

OBJECTIVES

- You will be able to state the function and size of the CPU operating registers.
- You will be able to state the function and size of the CPU support registers.
- You will be able to list the functions and registers in the serial CPU large arithmetic section and the small arithmetic section.

While viewing the microfiche, refer to the serial processor block diagram in figure 1-2.

At this time, locate the microfiche and audiotape titled, Serial Processor Block Diagram (microfiche 75444726, audiotape 75444710), load them, and proceed with the activity.

STUDENT NOTES

CYBER 170 Model 720/730 CPU
Learning Activity 1-C

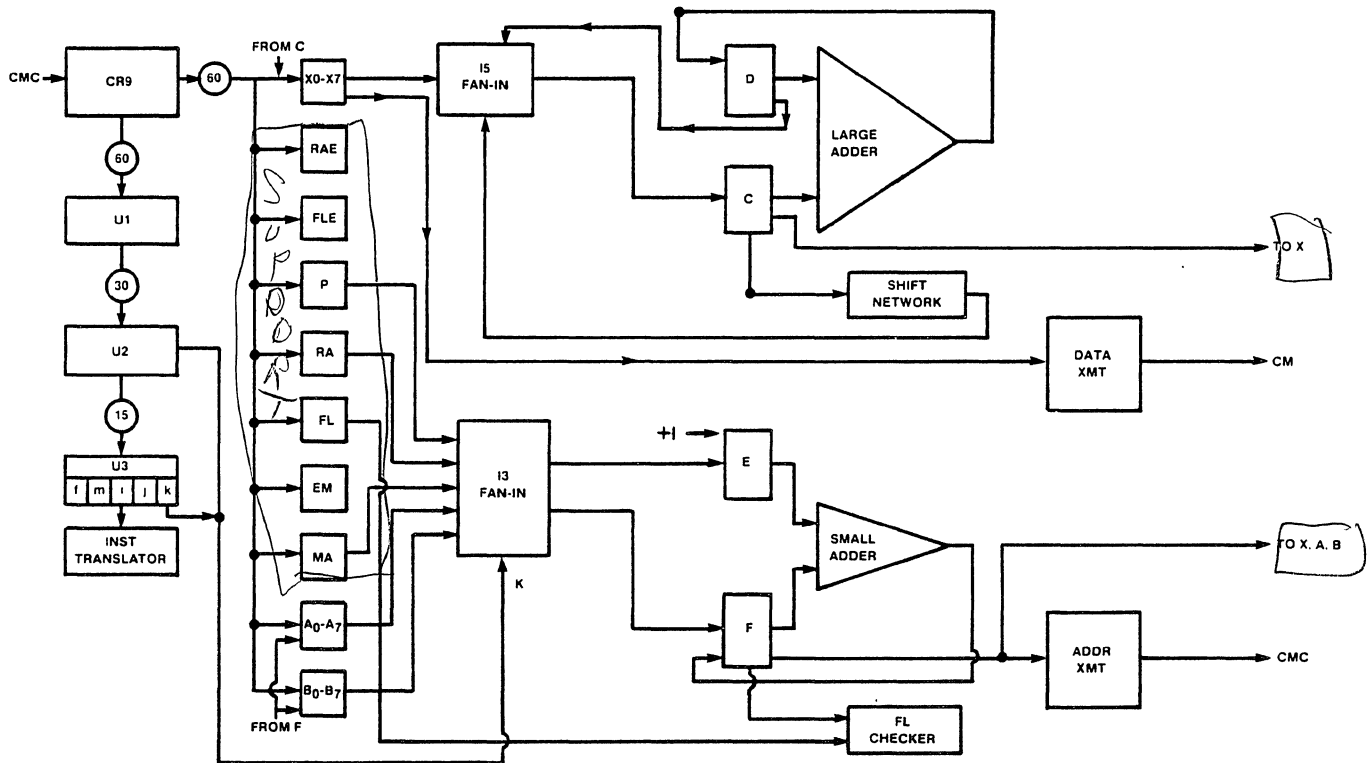


Figure 1-2. CYBER 170 CPU Block Diagram

Support - P RA FL MA EM
RAE FLE

CYBER 170 Model 720/730 CPU
Learning Activity 1-D

**LEARNING ACTIVITY 1-D. EXERCISE:
REVIEW OF CPU BLOCK DIAGRAM**

This activity reinforces what you learned about CPU functions in learning activities 1-B and 1-C. If you wish, you may review the microfiche in the previous activity while you are answering the questions in this exercise. For additional information on the CPU, read the following pages of the CYBER 170 Hardware Reference Manual, publication number 60456100, pages 2-3 through 2-7.

OBJECTIVES

- You will be able to state the functions the CPU services within a CYBER system.
- You will be able to state the function and size of the CPU operating registers.
- You will be able to state the function and size of the CPU support registers.
- You will be able to list the functions and registers in the serial CPU large arithmetic section and the small arithmetic section.

Directions: Complete the following statements by writing the most appropriate word or words in each blank.

1. The three types of operating registers in a CYBER CPU are called A, B, and X.
2. The CPU contains 8 X registers. Each X register contains 60 bits.
3. The operating registers that may be used as index registers are the B registers.
4. What is unique about operating register B0? Always 0
5. An instruction that used register A4 as the result register will initiate what action in the CPU? CPU READ
6. CPU registers A6 and A7 are scratch registers; if they are used as a result register, no memory reference is made. True or false? FALSE

CYBER 170 Model 720/730 CPU
Learning Activity 1-D

Directions: Match the following registers with their functions by placing the letter of the correct register in the blank.

	<u>Function</u>	<u>Register</u>
<u>D</u>	7. Program address register	a. FL
<u>A</u>	8. Number of CM locations available to current program	b. X5
<u>B</u>	9. 60-bit operand register	c. RAE
<u>h</u>	10. Lower limit of CM available to program	d. P
<u>F</u>	11. Defines which error conditions will cause an error exit	e. A3
<u>J</u>	12. Defines the number of ECS locations available to the CPU	f. EM
<u>i</u>	13. Only used if CPU can perform an exchange jump	g. B2
<u>E</u>	14. 18-bit address register	h. RA
		i. MA
		j. FLE

Directions: Complete the following statements by writing the most appropriate word or words in each blank.

15. All CPU addressing of central memory is done in a relative mode because a program may when results in a memory area.
16. The section of a serial processor CPU that handles all 60-bit arithmetic operations is called the large arithmetic.
17. The section of the CPU that performs 18-bit arithmetic functions is called the small arithmetic.

CYBER 170 Model 720/730 CPU
Learning Activity 1-D

Directions: In the blank preceding each of the listed registers, indicate which section of the CPU it is in or what type of register it is. Use the terms LAS, SAS, Operating, or Support.

	<u>Register</u>
<u>SAS</u>	18. F Register
<u>S</u>	19. RA register
<u>LAS</u>	20. D register
<u>LAS</u>	21. Shift network
<u>O</u>	22. X0-X7
<u>SAS</u>	23. E register
<u>S</u>	24. P register
<u>SAS</u>	25. I3 fan-in
<u>LAS</u>	26. C register
<u>O</u>	27. B0-B7

CYBER 170 Model 720/730 CPU
Learning Activity 1-D

The answers for this learning activity are on the following page.

CYBER 170 Model 720/730 CPU
Learning Activity 1-D

ANSWERS FOR LEARNING ACTIVITY 1-D

1. X, A, B
2. eight, 60
3. B
4. It is always set to zero.
5. A read of the CM address that is in A4. The operand the CPU receives from CM will be stored in register X4.
6. False; A6 and A7, are address registers used when storing data in CM. Register A0 is the only one of the eight registers that may be used as a scratch register.
7. d
8. a
9. b
10. h
11. f
12. j
13. i
14. e
15. The program may reside at any location in CM where there is room for it. This determination and assignment may be done by the monitor program of the operating system.
16. Large arithmetic section
17. Small arithmetic section
18. SAS
19. Support
20. LAS
21. LAS

CYBER 170 Model 720/730 CPU
Learning Activity 1-D

- 22. Operating
- 23. SAS
- 24. Support
- 25. SAS
- 26. LAS
- 27. Operating

LEARNING ACTIVITY 1-E. AUDIO/MICROFICHE: CPU INSTRUCTION AND OPERAND FORMAT

During this activity you learn the basic operand and instruction formats used in a CYBER system CPU. The operand and instruction formats are identical for all types of CPUs. This consistency makes the system's program compatible, which allows the customer to change from one type of system to another with minimal change in the software.

OBJECTIVES

- You will be able to define the instruction designators used in 15-bit and 30-bit CPU instructions.
- You will be able to list the three types of operand formats used in the CPU.
- You will be able to define the terms parcel and instruction word as they relate to CPU operations.

This activity refers to the instruction control registers of the serial type of CPU. These registers are shown on the same block diagram that you used during learning activity 1-C (figure 1-2). Refer to this block diagram while watching the microfiche.

At this time, locate the microfiche and audiotape titled, CPU Instruction and Operand Formats (microfiche 75444727, audiotape 75444711), load them, and proceed with the activity.

STUDENT NOTES

LEARNING ACTIVITY 1-F. EXERCISE: CPU INSTRUCTION AND OPERAND FORMAT REVIEW

This activity reinforces what you learned in learning activity 1-E about the CPU instruction and operand formats. If you wish, you may review the microfiche in the previous activity while you are answering the questions in this exercise. For backup information, read pages 4-3 through 4-4 of the CYBER 170 Hardware Reference Manual, publication number 60456100.

OBJECTIVES

- You will be able to define the instruction designators used in 15-bit and 30-bit CPU instructions.
- You will be able to list the three types of operand formats used in the CPU.
- You will be able to define the terms parcel and instruction word as they relate to CPU operations.

Directions: Complete the following statements by writing the most appropriate word or words in each blank.

1. The three basic operand formats of the CYBER CPU are 18 integers
and 60 bit floating point 60 bit integers.
2. The sign bit of an 18-bit operand is bit _____.
3. The advantage in expressing numbers in a floating point format is that a very large range of operands
may be manipulated.
4. The CPU has two basic instruction formats, they are the 15-bit instructions and the 30-bit instructions.

CYBER 170 Model 720/730 CPU
Learning Activity 1-F

Directions: Match the instruction designators with their bit positions by placing the letter of the correct bit position in the blank.

<u>Instruction Designator</u>	<u>Bit Position</u>
<u>E</u> 5. f	a. Bits 0-2
<u>D</u> 6. m	b. Bits 3-5
<u>C</u> 7. i	c. Bits 6-8
<u>B</u> 8. j	d. Bits 9-11
<u>A</u> 9. k	e. Bits 12-14

Directions: Complete the following statements by writing the most appropriate word or words in each blank.

- A CPU instruction code of 10123 says, "Transfer the contents of X_j to X_i." For this example, you will transfer the contents of X 2 to X 1.
- The contents of the lower 18 bits of a 30-bit instruction are an immediate operand.
- If a 30-bit instruction is a jump instruction, the large K of the instruction is the address.
- A CPU instruction word can contain up to 4 15-bit instructions.
- Each 15-bit byte of an instruction word is called a parcel.
- The CPU asks for the next instruction word after the completion of parcel 3 of the instruction word. True or false? False
- Fifteen-bit instructions and 30-bit instructions may be intermingled in one CPU instruction word. True or false? TRUE
- A 30-bit instruction in parcel 3 is legal if parcel 0 of the next instruction contains the lower 15 bits. True or false? False
- The serial processor instruction control registers are called U1, U2, and U3.
- The instruction translator in the CPU looks at the output of register U3.

CYBER 170 Model 720/730 CPU
Learning Activity 1-F

The answers for this learning activity are on the following page.

CYBER 170 Model 720/730 CPU
Learning Activity 1-F

ANSWERS FOR LEARNING ACTIVITY 1-F

1. 18-bit integer
60-bit integer
60-bit floating point
2. 2^{17}
3. The floating point format provides a processor with a much larger range of numbers or values to manipulate.
4. 15, 30
5. e
6. d
7. c
8. b
9. a
10. 2, 1
11. Immediate operand
12. Jump address
13. 4
14. parcel
15. False; the request is made after the execution of the instruction in parcel 0.
16. True
17. False; a 30-bit instruction in parcel 3 is always illegal.
18. U1, U2, U3
19. U3

LEARNING ACTIVITY 1-G. AUDIO/MICROFICHE: DATA FLOW

During this activity you learn how the CPU executes basic instructions and also how data flows through the CPU during accesses to central memory.

OBJECTIVES

- You will be able to trace data flow through the various sections and registers of a CPU block diagram during the execution of an instruction.
- You will be able to trace the address and data paths used during a reference to CM by the CPU.

Refer to the serial processor block diagram in figure 1-3 on the following page while you are watching the microfiche.

At this time, locate the microfiche and audiotape titled, Serial Processor Data flow (microfiche 75444728, audiotape 75444712), load them, and proceed with the activity.

STUDENT NOTES

CYBER 170 Model 720/730 CPU
Learning Activity 1-G

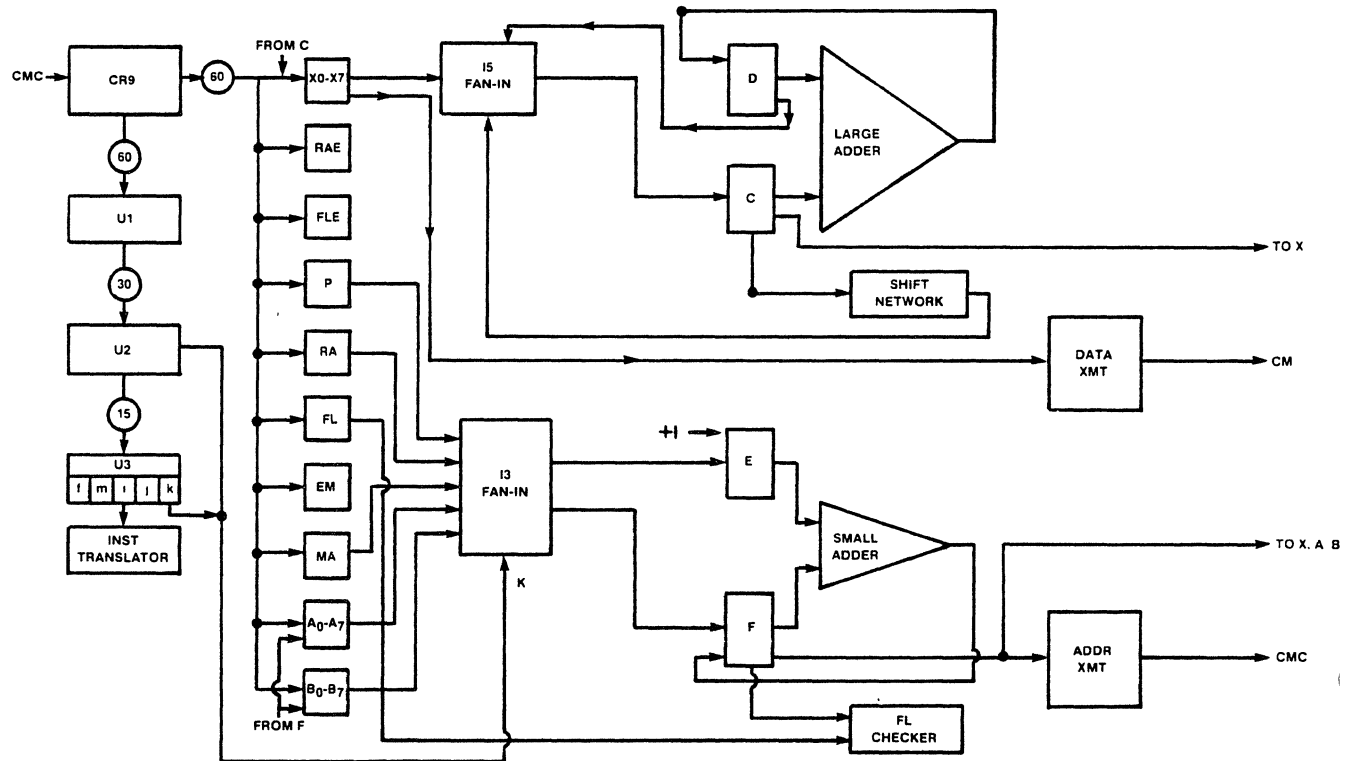


Figure 1-3. CYBER 170 CPU Block Diagram

LEARNING ACTIVITY 1-H. EXERCISE: DATA FLOW REVIEW

This activity reinforces what you learned about the operations of the serial processor during learning activity 1-G. If you wish, you may refer to the filmstrip in learning activity 1-G for review.

OBJECTIVES

- You will be able to trace data flow through the various sections and registers of a CPU block diagram during the execution of an instruction.
- You will be able to trace the address and data paths used during a reference to CM by the CPU.

Directions: Complete the following statements by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of this activity.

1. The path used to move an operand into the D register is X I5, C, LAS D.
2. The data path used to store a result operand from a D register into an X register is D I5, C, X.
3. A left shift of 10 places in the shift network takes 10 times as long as a left-of-one place. True or False? FALSE
4. A 20506 instruction says left shift X 5 by 6 places.
5. The data path used to load an operand from an A register into the E register is A, I3, E.
6. The results of any operation in the small adder are placed in the F register.
7. The Field Length check is made before RA is added to the relative address. True or false? TRUE
8. When performing a read of a CM location, the CPU must stop and wait until data is received before it starts the next instruction.
9. When writing data into CM, the operand to be stored must be in register X6 or X7.
10. An address parity error in a CYBER 170 system may cause the CPU to do an error exit.

CYBER 170 Model 720/730 CPU
Learning Activity 1-H

ANSWERS FOR LEARNING ACTIVITY 1-H

1. I5, C, large adder
2. I5, C, X
3. False; the shift network is a parallel shifter, therefore, all shifts can be performed in the same length of time.
4. 5, six
5. A, I3, E
6. F
7. True
8. the data is received
9. X6 or X7
10. error exit

LEARNING ACTIVITY 1-I. TEXT READING: CPU CHARACTERISTICS AND INTERFACES

During this activity you learn the characteristics of the CYBER 170, Models 720 and 730 CPUs. You also learn how the CPU is interfaced to CMC and to the ECS/ESM coupler.

OBJECTIVES

- You will be able to state the operational characteristics of the CYBER 170, Models 720 and 730 CPUs and the differences in the two models.
- You will be able to state how both CPU-0 and CPU-1 are interfaced to CMC and to the ECS/ESM coupler.

The Models 720 and 730 basic computer systems each have a serial CPU. The title for the basic CPU is CP-0. An option for the customer is a second CPU. If there is a second CPU in the system it is labeled CP-1.

CP-0 and CP-1 are functionally identical. Each has an arithmetic unit, instruction control section, and a compare/move unit. The only differences in CP-0 and CP-1 are in the area of interface to central memory control (CMC) and extended memory (EM). These differences are discussed later in this activity.

The CPU in a Model 720 system is functionally the same as the CPU in a Model 730 system. There is only one difference between a model 720 and a Model 730. That difference is the processing speed of the two models. The Model 730 runs at maximum speed. The Model 720 runs slower by 350 nanoseconds per instruction executed. This lower speed is accomplished by putting a delay between the exit from one instruction and the beginning (RNI) of the next instruction's execution. In the Model 730 there is no delay between instructions.

For further information on the characteristics and functional descriptions of the Models 720 and 730, you should read the System Description (section 1) and the Functional Description (section 2) of the CYBER 170 Computer Systems Reference Manual, publication number 60456100.

The instruction set that can be executed by the Models 720 and 730 CPUs are identical. The execution time of the instructions varies with the type of instruction. Refer to table 4-3, CP Instruction Timing, in the CYBER 170 Reference Manual for a listing of all instruction execution times.

CYBER 170 Model 720/730 CPU
Learning Activity 1-I

CP-0 of the Model 720 and 730 is located in chassis 1 of the mainframe bay. CP-1, if present, is located in chassis 4. Also located in chassis 1 is the central memory control (CMC) section of the system. If the mainframe has any extended memory (EM) connected to it, the coupler to it is located in chassis 4.

The differences in the content of chassis 1 and 4 causes some differences in the transmission parity scheme for the two CPUs. Transmission parity generation/checking is performed only when signals are transmitted between two chassis. Therefore, there is no parity checking between CP-0 and CMC, nor is there parity checking between CP-1 and the EM coupler. There is parity checking on data and addresses between CP-1 and CMC, and also between CP-0 and the EM coupler.

Refer to figure 1-4 for a visual description of the relative locations and interfaces of the CPUs in the CYBER 170 Models 720 and 730 systems.

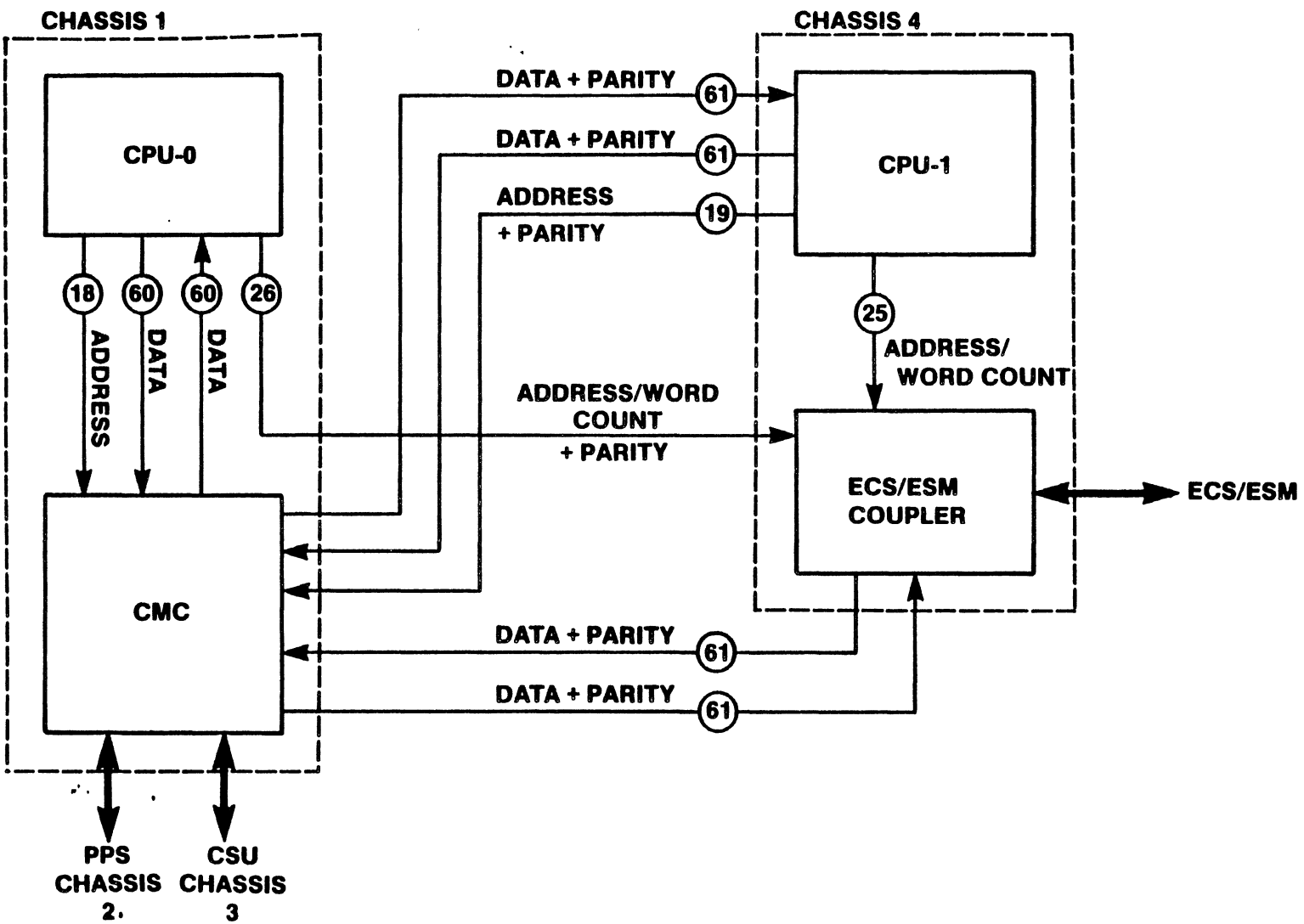


Figure 1-4. CYBER 170 Models 720, 730 CPU/CMC Interface

CYBER 170 Model 720/730 CPU
Learning Activity 1-I

SUMMARY

During this activity you have learned some of the operational and functional characteristics of the CYBER 170 Models 720 and 730 CPU and the differences of the two models. Also you have learned how CP-0 and CP-1 interface to the CMC and EM coupler sections of the mainframe.

If you wish, you may review this activity before proceeding to the next lesson in your assignment.

LEARNING ACTIVITY 1-J. TEXT READING: DETAILED BLOCK DIAGRAM

During this activity you learn the layout of the CYBER 170, Models 720 and 730 CPU at a detailed block diagram area.

OBJECTIVES

- You will be able to identify the registers that are included in each major section of the CPU.
- You will be able to follow data paths through the CPU on a detailed block diagram.
- You will be able to locate each section of the detailed block diagram in the CPU diagrams manual.

INTRODUCTION

All references in this activity refer to the CYBER 170 Models 720 and 730 CPU detailed block diagram found in figure 1-5. At this time, locate the block diagram and fold it out so that you can refer to it more easily while reading this text.

The block diagram shows all the major blocks and registers in the CPU. Note that it does not show the compare move unit (CMU) section of the CPU. The CMU block diagram will be covered during a later module in this course.

The block diagram is divided into four sections: instruction control, large arithmetic section, small arithmetic section, and output section. The elements of each section will be described and then general data flow will be explained.

Note that each block on the diagram has a name which identifies its function or its title as it appears in the logic diagrams. In the upper left corner of each block is a small box with two letters in it. These two letters are the module type as identified in the CPU mainframe and in the logic diagrams. This will help you to locate the register or element in the logic diagrams.

Just above each block is the page number in logic diagrams where you can find the logic for that element. This helps you to find the detailed logic for any element quickly.

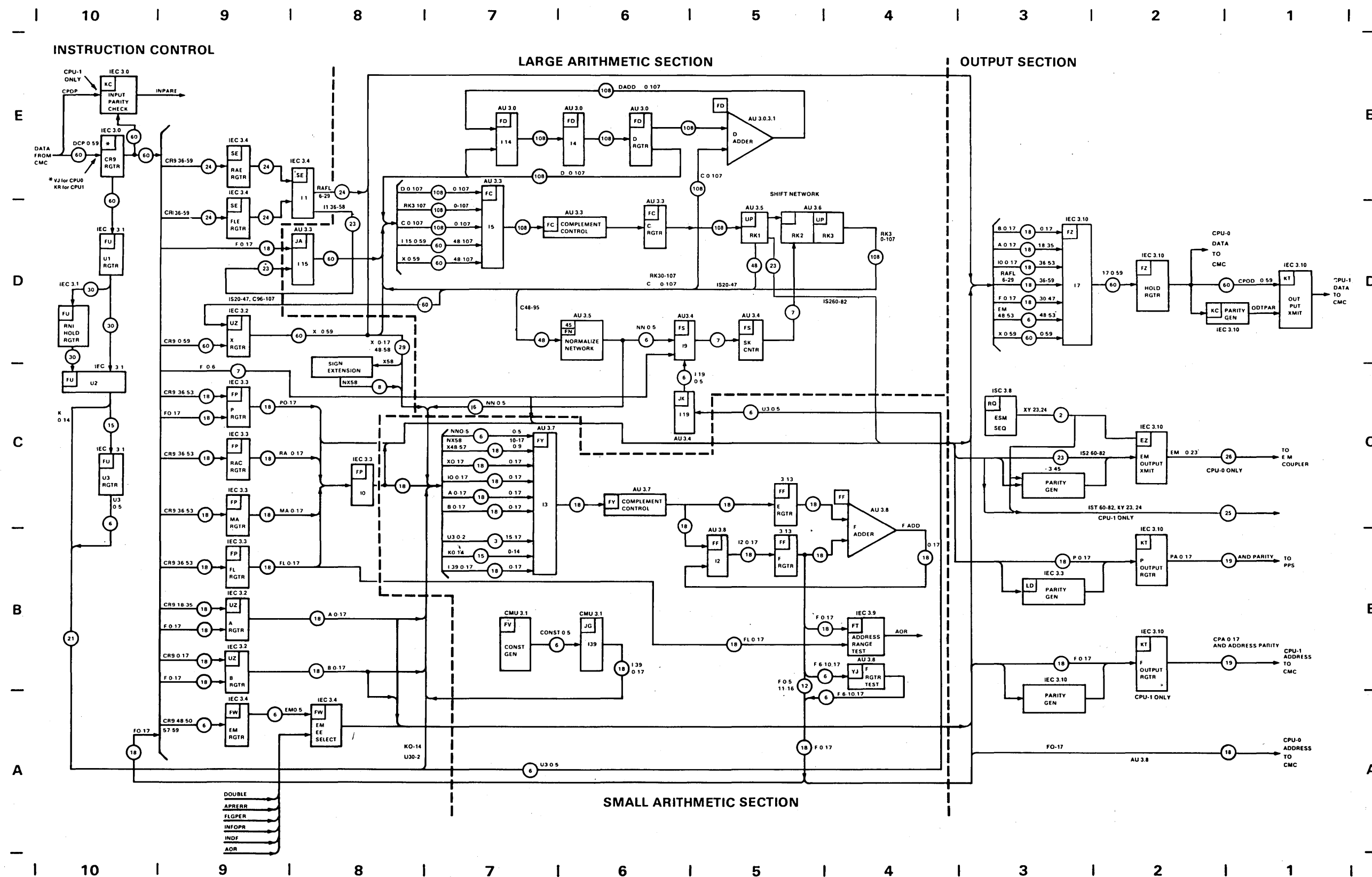


Figure 1-5. CYBER 170 CPU Block Diagram

INSTRUCTION CONTROL

The instruction control section of the block diagram contains the input data from CMC (CR9), the instruction control registers (U1, U2, U3, and RNI Hold), the CPU's operand registers (X, A, and B), and the support registers (RAE, FLE, P, RAC, MA, FLC, and EM).

All data coming into the CPU enters through the CR9 register (page co-ordinate E10). CR9 is a 60-bit register. Note that there are two module types identified in the block. The type is dependent on which CPU (0 or 1) you are referencing. In CPU-0 the VJ modules are used. In CPU-1 the KR modules are used and, also, the input parity check circuit (KC module) is used in CPU-1. As you recall, CPU-0 is in the same chassis as CMC. Therefore, there is no parity on the lines between CMC and CPU-0. CPU-1 is in a different chassis, so there is parity checking on data it receives from CMC.

The data in CR9 can be an instruction word, an exchange package word, or a 60-bit operand. If it is an instruction word it will be sent to register U1. If the data is an exchange package word it will be gated to the appropriate support registers and/or operand registers. If the data in CR9 is a 60-bit operand it is always gated to an X register.

The instruction registers U1, U2, U3, and RNI Hold are used to hold the instruction word and control the parcelling of each instruction to U3. The U3 register holds the instruction currently being executed by the CPU. Its contents are decoded and signals are generated to start the correct instruction sequence and gate register contents to the required sections of the CPU. The basic operation of U1, U2, U3, and RNI Hold were covered in a previous activity. You review that activity if you wish.

The operand registers X, A, and B each have two inputs. One input is from CR9 and the other is from the arithmetic sections of the CPU. The inputs to the A and B registers from CR9 are used only during an exchange jump sequence. This is to load the registers initially. The other input to A and B is from the F register. This input is used to store the results of any instruction which uses A or B as its result register (5X or 6X instructions for example).

The CR9 input path to the X registers is used during both an exchange jump and when the CPU does a read of CM. The exchange jump loads X with an initial operand. The central memory read occurs whenever the program executes a 5X instruction and the i portion of the instruction is equal to one through five.

The other input to the X registers is from the large arithmetic section. This path is used to store the results of any instruction

CYBER 170 Model 720/730 CPU
Learning Activity 1-J

which designates X as its result register (1X, 2X, 3X, 4X and 7X instructions). The upper 12 bits of X (bits 48-59) come from bits 96-107 of the C register.

The lower 48 bits of X (bits 0-47) come from rank 1 of the shift network (IS2 0-47). This is to accommodate both single and double precision instruction results. For single precision instructions, bits 48-95 of the C register go to rank 1, get shifted right 48 places and then go to the X register. For double precision instructions, bits 0-47 of the C register are gated straight through Rank 1 with no shifting and then transmitted to the X register. Using rank 1 of the Shift Network eliminates the need for additional gating circuits on the input to the X registers.

The output of the X registers go to several places. The output to I7 is used during exchange jump and whenever data is to be stored in CM as an operand. Another output from X goes to I5 and is used whenever the operand is to be used in the large arithmetic section. Portions of X also go to the small arithmetic section (SAS) for use by certain instructions. Bits 0-17 of X go to I3 and into the SAS during increment instructions (5X, 6X, or 7X). Bits 48-59 of X go to I3 and into the SAS for use during floating point operations. The upper 12 bits of X are the exponent and sign bits of a floating point operand and exponent manipulation is performed in the SAS.

The A register outputs go to the SAS through I3 for arithmetic manipulation. The other output from the A registers goes to I7 and is used only during an exchange jump to store the results of the A registers in the output exchange package in CM.

The output from the B registers goes to I3 and into the SAS for arithmetic operations. B register outputs to I7 are only used during an exchange jump to store B register contents in the output exchange package area of CM.

Except for the P register, the only inputs to the support registers is from CR9. This is because the support registers are loaded during an exchange jump and their contents do not change during the execution of a program in the CPU. The P register has an input from the F register in the SAS. This input is used to update the P register during an RNI or to set a jump (branch) address into P. The updated P register contents (P+1) or the jump address is formed in the SAS and then stored in P.

The output of the P register goes three places. It goes to I0 and then to I3 as input to the SAS. This path is used whenever P is to be changed (updated). The second destination of P output is to the P Output register (coordinate B2). This path is used to transmit the content of P to the PPS chassis. This content of P is transmitted every 50 nanoseconds and can be read by a PP by using the 270X PP

instruction. The third output path from P is to register I7. This path is used during an exchange jump to store the contents of P in the output exchange package area in CM. The P to I7 path is also used to store P in CM during a return jump instruction sequence.

The output of the RAC register goes through I0 and then to I7 for storage in the CM output exchange package. The output of RAC through I0 also goes to the SAS and is used to form absolute CM addresses by adding it to a relative address which has been formed in the SAS.

The output of the MA register also goes through I0 and then to I7 for exchange jump storage. The MA output through I0 also goes to SAS for use during a central exchange jump instruction sequence.

The FLC register output path is through I0 to I7 for exchange jump output storage. FLC contents are also used in the address range test circuit (coordinate B4) to compare a CM address formed in the F register with the program's field length. If the address in F is greater than the content of FLC, a address out of range (AOR) condition will exist.

The EM register outputs to the EM/EE select circuit (coordinate A8). The content of the EM register is compared to the six error conditions that the CPU checks. If a match of an EM bit and an error exit signal exists an error exit condition exists and the CPU control circuitry will be notified. Based on various conditions, the CPU may then do an error exit from the program it is currently executing. An error exit may mean the CPU stops or it may cause the CPU to do an exchange jump to a monitor type of program. The output of the EM/EE Select register may be the content of the EM register, which will go to I7 for storage during an exchange jump.

The other output of the EM/EE select is the error exit condition bits which caused the error to occur. This output will go to I7 for storage in address RA as a part of the error exit sequence results.

The outputs of RAE and FLE registers are gated through I1. The output of I1 goes to I7 for storage of RAE and FLE in CM during an exchange jump. The other output from I1 goes to I15 and then into the large arithmetic section (LAS). This path is used when the CPU is performing an extended memory transfer instruction (011 or 012). The RAE and FLE contents are used to form and check EM addresses in the LAS.

At this time you should carefully study the block diagram to ensure that you can find and follow all inputs and outputs of the registers in the instruction control section.

CYBER 170 Model 720/730 CPU
Learning Activity 1-J

OUTPUT SECTION

The output section of the CPU block diagram contains all the output paths from the CPU to other sections of the CYBER mainframe. Some of these registers have already been referenced in this lesson.

The I7 and Hold register circuits provide the path for all data going to CM. I7 is simply a fan-in gating register which enables the outputs of various CPU registers to be gated to the output circuits. The Hold register holds the data word for one clock time before it is transmitted to CMC.

In CP-0 the output of the Hold register goes directly to CMC. No parity is generated because CP-0 and CMC are on the same chassis.

In CP-1 the output of the Hold register goes to a parity generator and then the parity bit and the 60 data bits are transmitted from the KT modules in chassis 4 to CMC in chassis 1.

The data going through I7 and the Hold register may be exchange package data or it may be an operand to be stored in CM. All I7 inputs are used during an exchange jump sequence. Only the X register input to I7 is used when storing an operand in CM.

Addresses from the CPU to CMC come from the F register in the SAS. In CP-0 the address is sent directly to CMC from F with no parity generated. In CP-1 the output of F goes to a parity generator (coordinate A3) and then the parity bit and F contents are transmitted to CMC from the F Output register.

The P Output register (coordinate B2) is used to transmit the content of the CPU's P register to PPS chassis. Because the PPS is in a different chassis a parity bit is also transmitted. The output of P to the PPS is unconditional. That is, as long as power is applied to the mainframe the CPU will transmit the content of its P register to the PPS every clock time. It is a function of a PP program to input Central P address if it wants to examine where the CPU program is at.

The last part of the output section is to the EM coupler which is located in chassis 4. The CPU must send a word count and address to EM before a transfer can occur. The word count and address are formed in the C register and then are sent through rank 1 of the shift network as bits IS2 60-82. These bits go directly to the EM coupler in CP-1 as they are on the same chassis. In CP-0 IS2 60-82 go through a parity generator (coordinate C3) and then are transmitted along with the parity bit from the EM Output Xmit register to the EM coupler.

If the system has extended semiconductor memory (ESM) connected to it, there are two more bits sent along with IS2 60-82. These bits are generated in the ESM sequence (coordinate C3) and are transmitted at the same time as the other bits are. They are included in the parity generator from CP-0.

This concludes the description of the output section of the CPU detailed block diagram. You should be able to follow data paths from the input to the CPU to its output at this time.

LARGE ARITHMETIC SECTION

The LAS is used to perform operations on all 60-bit operands in the CPU. The principal elements of the LAS are the D adder, the shift network, and the normalize network. The two prime registers are the C register and the D register.

All inputs to the LAS come in through I5. I5 is an eight input fan-in circuit. The data inputs to I5 are from the D register (108 bits), the shift network (108 bits), the C register (108 bits), I15 (60 bits), and the X registers (60 bits). In addition, there are three octal constants that can be generated within I5. They are 0₈, 4₈, and 6₈. These constants are used by various instruction sequences to form parts of operands in the LAS.

The inputs to I5 are selectable by bit position. That is, portions of more than one input register can be gated at the same time. For example, bits 0-47 can be forced to a constant 0₈ while bits 48-95 are gated from the C register, and bits 96-107 come from I15. This way operands can be formed at the output of I5 more easily than if separate or additional registers were used.

The output of I5 goes through the complement control circuit. In complement control all or portions of the I5 output may be complemented. This feature is used often in the CPU. For example, in order to subtract one operand from another, one operand will be complemented and then the two values are added to find the difference.

The output of I5 and its complement control goes only to the C register. The output of the C register goes several places. It goes to the D adder, the shift network, and the normalize network.

The input from the C register to the D adder is the only path to get an operand into the D register. The entire path is from C through the adder (add C to zeros, so no change), through I14, then I4, and finally into the D register. This concept was explained in a previous activity.

CYBER 170 Model 720/730 CPU
Learning Activity 1-J

The path to get an operand from D back to C is from D through I5 and then to C.

The output of the D adder goes only to I14. From I14 it goes to I4 and then into D. I14 is a fan-in which selects either the output of the adder or the output of D to be gated through. The path from D through I14 and I4 and back to D is used during certain conditions of a multiply or divide sequence. You will learn more about that in future lessons.

I4 is called the iterative shifter. This means that it can shift its output one place from its input. Three operations are possible: shift one place to the right, shift one place to the left, or no shift. The shift feature in I4 is used during floating multiply, divide, and add sequences and also the pop count sequence. You will see its operation when you study those sequences later.

The input to the shift network (SN) comes from the C register. The SN performs parallel shifts of its input operands. The number of places to be shifted is held in the SK CNTR (shift counter). The direction of the shift, left or right, is determined by the instruction being executed. Right shifts are end-off with sign extension in the upper bits. Left shifts are end-around from bit 48 to bit 107. The lower 48 bits (0-47) of the SN are not used during a left shift. The output of rank 3 of the SN goes to I5 and then into the C register.

SN rank 1 output is used as the path to the X registers to store the results of an instruction. This concept was explained previously in this lesson. Also you learned that RK1 output goes to the EM coupler output section during an EM transfer.

Bits 48-95 of C feed the normalize network (NN). The NN determines the bit position of the most significant digit of a floating point operand and generates a count which is the difference between its position and the highest position (2^{47}). This difference becomes a shift count which is loaded into the SK CNTR. The operand in C then gets left-shifted that number of places. This moves the most significant bit of the operand's coefficient into bit 47 of the operand. At the same time the normalize count is transmitted to the SAS and is subtracted from the operand's exponent to retain the true value of the operand.

There are two other inputs to the shift counter register. U3, bits 0-5, go through I19 and I9 and then into the SK CNTR. These bits are the j and k portion of the instruction and they are the shift count for the 20 and f21 CPU instructions.

The last SK CNTR input is through I9. It comes from bits 0-7 of the F register. This shift count is used during 22 and 23 (nominal shift) instructions and during a floating add or difference sequence to equalize the coefficients.

The last register to be discussed in the LAS is I15. I15 serves as the interface from the SAS to the LAS. During a 7X instruction an 18 bit result is formed in the F register. The result must be stored in a X register so bits 0-17 of F go to bits 0-17 of I15. Then from I15 they go to I5 with sign bits in bit positions 18-59. The operand then goes to C, through RK1 and into the X register.

During floating point instruction sequences the exponents are manipulated and/or formed in the SAS. When the final operand is to be formed in the LAS, the exponent in bits 0-10 of F is sent to bits 48-58 of I15. The coefficient sign bit is added to bit 59 of I15 and then the 12 exponent and sign is gated through I15 to I15 bits 96-107 at the same time the coefficient is gated through bits 0-95 of I5.

The other input to I15 is from I1 and is used during the execution of an EM transfer (011, 012) instruction.

This concludes the description of the LAS section of the CPU block diagram. Practice following the several paths through the LAS.

SMALL ARITHMETIC SECTION

The small arithmetic section is used during almost every instruction sequence the CPU executes. It is also used during a read next instruction (RNI) to update the contents of the P register.

The principal element of the SAS is the F adder. The inputs to the F adder are the E register and the F register. All results from the F adder go through I2 and into F register.

All inputs to the SAS come in through I3. I3 is nine input fan-in circuit. The appropriate input is gated by control circuits. The instruction sequences determine when and which inputs to I3 are selected. The output of I3 goes through the complement control circuit and then to either E or through I2 to F. The instruction sequence determines which path is used.

All outputs from the SAS leave from the F register. The F register goes to the: A registers, B registers, Address Range Test circuit, CMC (CM address), I7, LAS (I15), P register, and Shift Count register (through I9).

CYBER 170 Model 720/730 CPU
Learning Activity 1-J

As you go through various instruction sequences you will see how and when the SAS is used.

This completes the description of the CYBER 170 Model 720 and 730 CPU detailed block diagram. If you wish, you may review any of the descriptions before proceeding to your next activity.

LEARNING ACTIVITY 1-K. EXERCISE: CPU CHARACTERISTICS

This activity reinforces what you learned about the CPU characteristics and the detailed block diagram in learning activities 1-I and 1-J.

OBJECTIVES

- You will be able to state the operational characteristics of the CYBER 170, Models 720 and 730 CPUs and differences in the two models.
- You will be able to state how both CPU-0 and CPU-1 are interfaced to CMC and to the ECS/ESM coupler.
- You will be able to identify the registers that are included in each major section of the CPU.
- You will be able to follow data paths through the CPU on a detailed block diagram.
- You will be able to locate each section of the detailed block diagram in the CPU diagrams manual.

Directions: Refer to learning activities 1-I and 1-J and pay particular attention to the figures 1-4 and 1-5. Answer the following questions writing the most appropriate word or words in each. Compare your answers to those given at the end of this activity.

1. The title for the basic CPU for the Model 720, 730 is CPU-0.
2. The Model 720 CPU runs 350 nanoseconds per instruction slower faster than the model 730 CPU.
3. CPU 0 is located in chassis 1.
4. CPU 1 is located in chassis 4.
5. CMC is located in chassis 1.
6. Parity checking _____ is is not required between CPU-0 and CMC.

CYBER 170 Model 720/730 CPU
Learning Activity 1-K

7. The four sections of the CPU detailed block diagram are LAS, SAS, instruction control, and output section.
8. List the instruction control registers U1, U2, U3, RNT HOLD.
9. List the CPU operand registers A, B, X.
10. List the CPU support registers RAE, FLA, RAC, FLC, P, MA, and EM.
11. On which detailed-pak diagram is the Shift Network Ranks 2 and 3 located? AU 3.6
12. On which detailed-pak diagram is the F ADDER located? AU 3.8
13. On which detailed-pak diagram is the A register located? IEC 3.2
14. Which bits of the X register are available to I3? X0-17 X48-58

CYBER 170 Model 720/730 CPU
Learning Activity 1-K

The answers for this learning activity are on the following page.

CYBER 170 Model 720/730 CPU
Learning Activity 1-K

ANSWERS FOR LEARNING ACTIVITY 1-K

1. CPU 0
2. 350 nanoseconds; slower
3. .1
4. 4
5. 1
6. is not
7. Instruction Control; Large arithmetic; Small arithmetic;
and Output
8. U1, U2, U3, RNI HOLD
9. X, A, B
10. REA, FLE, P, RAC, MA, FLC and EM
11. AU 3.6
12. AU 3.8
13. IEC 3.2
14. X0-17; X48-58

POST TEST

When you have completed the learning activities assigned for module 1, sign on to the PLATO terminal and take the module 1 test.

Depending on the results of the test, you will be told to either review some of the previous activities, or to go on to module 2.

MODULE 2

INSTRUCTION EXECUTION CONTROL (IEC) LOGIC

During this module you learn to follow data paths and control signals through the logic diagrams included in the IEC section of the CPU diagrams manual. You also learn how the clock signals that control CPU operations are generated.

PRETEST

To start this module, sign on to the PLATO terminal and read the objectives. If you feel that you might be able to meet some of the objectives, take the module test. After evaluating the results of your test, PLM will assign the learning activities that relate to the objectives you did not meet. If you do not wish to take the test first ask for an assignment.

LEARNING ACTIVITIES

In the assigned column, put a check mark by each activity assigned to you by PLM. Then proceed through your assigned activities. Check off each activity as you complete it. You may choose to do all the activities or do some activities more than once.

<u>Assigned</u>	<u>Completed</u>	<u>Activity</u>	<u>Description</u>	<u>Page</u>
_____	_____	2-A	Reference Reading: Diagrams Manual Overview. This learning activity provides an overview of the usage of the hardware maintenance manual.	2-3
_____	_____	2-B	Exercise: Diagram Manual Overview. This learning activity reinforces what you learned about the hardware maintenance manual usage.	2-7
_____	_____	2-C	Reference Reading: CPU Clock. This activity covers the CPU clock.	2-11

CYBER 170 Model 720/730 CPU
Module 2

<u>Assigned</u>	<u>Completed</u>	<u>Activity</u>	<u>Description</u>	<u>Page</u>
_____	_____	2-D	Reference Reading: IEC 3.0 Theory of Operation. This learning activity covers the theory of operation for IEC 3.0.	2-12
_____	_____	2-E	Exercise: IEC 3.0 Theory of Operation Review. This learning activity reinforces what you learned about IEC 3.0.	2-13
_____	_____	2-F	Reference Reading: IEC 3.1 Theory of Operation. This learning activity covers the theory of operation of IEC 3.1.	2-15
_____	_____	2-G	Exercise: IEC 3.1 Theory of Operation Review. This learning activity reinforces what you learned about IEC 3.1.	2-16
_____	_____	2-H	Reference Reading: IEC 3.2 Theory of Operation. This learning activity covers the theory of operation of IEC 3.2.	2-19
_____	_____	2-I	Exercise: IEC 3.2 Theory of Operation Review. This learning activity reinforces what you learned about IEC 3.2.	2-20
_____	_____	2-J	Reference Reading: IEC 3.3 and 3.4 Theory of Operation. This learning activity covers the theory of operation of IEC 3.3 and 3.4.	2-23
_____	_____	2-K	Exercise: IEC 3.3 and 3.4 Theory of Operation Review. This learning activity reinforces what you learned about IEC 3.3 and 3.4.	2-24

LEARNING ACTIVITY 2-A. REFERENCE READING: DIAGRAMS MANUAL OVERVIEW

This learning activity introduces you to the CPU diagrams manual, its content, and the layout of the logic diagrams.

OBJECTIVES

- You will be able to identify the four basic sections of the logic diagrams.
- You will be able to locate the logic diagram for each block identified in the detailed block diagram of the CPU.
- You will be able to locate the pages of the theory of operation section that explain the operation of each diagrams page.

Directions: Locate your copy of the CDC CYBER 170 Models 720,730 Central Processor Unit Hardware Maintenance Manual, publication number 60456170. Then read the following and follow the directions given.

The CPU diagrams are divided into four basic sections. The title of each section and its abbreviation is:

- Instruction execution control (IEC)
- Arithmetic unit (AU)
- Instruction sequence control (ISC)
- Compare move unit (CMU)

The title of each section is a good description of the function of the logic included in it.

Each logic section has two levels of diagrams. They are level one and level three. Level one diagrams are called primary block diagrams (PBD); level three diagrams are called detailed pak diagrams. The CPU manual does not have any level two diagrams (secondary block diagrams).

There are level four diagrams available for the CPU. Level four diagrams are logic diagrams of each module type in the CPU. The CPU's level four diagrams are not included in the hard copy manual. They are found in the microfiche version of the CPU diagrams manual.

CYBER 170 Model 720/730 CPU
Learning Activity 2-A

Its publication number is 60456170. Generally, you will not have to reference the level four diagrams during this course. You normally can isolate CPU failures using the level three diagrams.

The hardcopy manual you have is a copy of the microfiche version of the CPU manual. It has been found that it is easier to use hardcopy of logic diagrams and theory of operation than to use a microfiche version. Because of this, the page numbering scheme may sometimes be confusing to you. The microfiche coordinates are still on each page, and not all pages have numbers. You will be directed to pages with the most logical identifier on that page.

At this time, locate the primary block diagram for the instruction execution control section. It is referenced in the lower right hand corner as IEC 1.0. Its microfiche coordinate is 40B1B2.

The 1.0 diagram shows the basic relationship between the various logical components comprising the functional entity, in this example, the IEC section. Note that it also shows the interfaces to the other parts of the CPU as well as interfaces to CMC and the PPS. Each section of the diagrams has a 1.0 diagram.

Now turn to the next page in the diagrams manual. This is the first page of 3.X level diagrams for the IEC section. This is the most explicit level of block diagram on the CPU. It gives a simplified block diagram of each unique pak and key test points.

The title block in the lower right corner of the page gives you the sheet number and the description of the function of the logic elements on the page. The sheet number is used to follow signals from one page to another.

At this time look at each page of the IEC section diagrams. Note the title of each page to become familiar with the content of this section. As you look at each page you should also reference the detailed block diagram of the CPU in figure 1-5. This will help you keep the big picture of the CPU as you examine the detailed diagrams. After you have looked at each IEC page, return here and continue your reading.

The next section of the CPU diagrams is the arithmetic unit (AU). Locate the page numbered AU 1.0 in your diagram. This is the primary block diagram of the AU section.

Now examine briefly the content of each 3.X DPD of the AU section. Relate the contents of each page to the CPU block diagram in figure 1-5. After you have become familiar with these pages, return here and continue reading.

Following the AU section, you find the instruction sequence control (ISC) section. The logic in this section is what controls the execution of the various instructions in the CPU. Locate the ISC primary block diagram; ISC 1.0.

Now, examine the content of each ISC 3.X page. Note the instructions which are controlled by each page. When you have completed your review of the ISC section, return here and continue reading.

The last section of the CPU diagrams includes the logic for the compare/move unit (CMU). At this time, locate the CMU diagrams in the manual. Briefly look at each page to note its content. When you are ready, return here and continue reading.

The clock distribution logic for the CPU is on its own separate page. The sheet number for this logic is CLK 3.0. It is found in your manual immediately after the last page of CMU diagrams. At this time, locate page CLK 3.0 in your CPU manual.

The next section of the CPU manual is the theory of operations. Each page of DPDs has a written theory of operations, which describes the functions of the logic on the page.

In your manual, locate the theory of operation for the IEC 1.0 PBD. It has a microfiche label of 43B1 and its page number is 1. (It is the next page in the manual following CLK 3.0.)

Notice that the title line includes both the sheet number (IEC 1.0) and the microfiche coordinate (40B2). This is to assist in cross-referencing the theory to the logic diagrams. If you refer to page IEC 1.0 you will find the microfiche coordinate there for its theory of operation. This way you are able to work both directions between the logic diagrams and the theory of operation section.

At this time, you may briefly page through the theory of operations section. When you have finished, return here and continue reading.

The last part of the CPU manual for you to examine is the instruction flow diagrams section. This section is actually appendix A of the manual. The entire appendix is figures numbered A-1 through A-45.

At this time, locate the instruction flow diagram section in your manual. The microfiche coordinate for the first page in the section is 50 B1 B2. (It is immediately after page number 156.48 of the theory of operations section.) The first instruction flow diagram is for initial start RNI and is figure A-1.

CYBER 170 Model 720/730 CPU
Learning Activity 2-A

The instruction flow diagrams give you a time/event relationship for each instruction or control sequence the CPU may execute. They are extremely useful to learn and to troubleshoot the CPU. You will be using these diagrams frequently during this course.

At this time, page through appendix A and note which sequences are represented by each page. When you have finished, return here and continue reading.

This completes the introduction to the CPU diagrams and theory of operation manual. You should now be able to locate the logic for the various CPU elements and locate the theory of operation for a given logic diagram. When you are ready, you may proceed to your next assigned learning activity.

LEARNING ACTIVITY 2-B. EXERCISE: DIAGRAMS MANUAL OVERVIEW REVIEW

This activity gives you practice in locating logic diagrams, theory of operations section, and instruction flow diagrams in the CPU diagrams manual.

OBJECTIVES

- You will be able to identify the four basic sections of the logic diagrams.
- You will be able to locate the logic diagram for each block identified in the detailed block diagram of the CPU.
- You will be able to locate the pages of the theory of operation section that explain the operations of each diagrams page.

Directions: Locate your copy of the CDC CYBER 170 Models 720,730 Central Processor Unit Diagrams manual, publication number 60456170. You will also use the CPU detailed block diagram, figure 1-5 of this student manual during this exercise.

Complete the following statements by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of the activity.

1. The four basic sections of the CPU diagrams are:

- a. instruction sequence control ISC
- b. arithmetic unit AU
- c. compare move unit CMU
- d. instruction execution control

2. Page ISC 1.0 is an example of a A.

- a. Primary block diagram
- b. Detailed pak diagram

CYBER 170 Model 720/730 CPU
Learning Activity 2-B

3. Match the elements of the CPU on the left with the section of logic it appears in from the right.

<u>2</u>	a. D adder	1. IEC
<u>1</u>	b. U1 register	2. AU
<u>2</u>	c. I3 fan-in	3. ISC
<u>3</u>	d. Shift instruction control	4. CMU
<u>4</u>	e. Compare/move hardware	
<u>1</u>	f. RNI sequence	
<u>1</u>	g. I7 output circuit	
<u>1</u>	h. P register	
<u>3</u>	i. Boolean instruction control	
<u>2</u>	j. Shift network	

4. What is the page number of the logic for each of the following CPU elements:

a. CR9 register	<u>IEC 3.0</u>
b. F adder	<u>AU 3.8</u>
c. I15 register	<u>AU 3.3</u>
d. X registers	<u>IEC 3.2</u>
e. Address out of range sequence	<u>IEC 3.9</u>
f. C register	<u>AU 3.3</u>
g. Return jump sequence	<u>ISC 3.0</u>
h. Compare move collate sequence	<u>CMU 3.15</u>
i. Clock distribution	<u>CLK 3.0</u>
j. Common time sequence	<u>IEC 3.7</u>

5. a. What is the DPD page number for the logic which controls the normalize instruction execution?

ISC 3.3

- b. What are the codes for the other instructions controlled by the same sequence?

20-23 24-27
43

6. What is the page number and microfiche coordinate of the theory of operation for the MA register?

a. Page number	<u>12</u>
b. Microfiche coordinate	<u>43C6</u>

7. Reference the theory of operation section, . page 26. What is the DPD page number of the logic described on this page? IEC 3.10

8. a. What is the figure number in appendix A of the instruction flow diagram for the increment sequence 36 and 37 instructions? A-13
- b. What is the DPD page number of the logic that controls the 36 and 37 instructions? FSC, 3, 7
- c. What is the page number in the theory of operations section that explains the Increment Sequence?
111 - 119

This concludes the exercise on introduction to the CPU diagrams and theory of operation manual. If you wish, you may review this activity and also learning activity 2-A before proceeding to the next activity.

CYBER 170 Model 720/730 CPU
Learning Activity 2-B

ANSWERS FOR LEARNING ACTIVITY 2-B

1. a. Instruction execution control (IEC)
 b. Arithmetic unit (AU)
 c. Instruction sequence control (ISC)
 d. Compare move unit (CMU)
2. a
3. a. 2
 b. 1
 c. 2
 d. 3
 e. 4
 f. 1
 g. 1
 h. 1
 i. 3
 j. 2
4. a. IEC 3.0
 b. AU 3.8
 c. AU 3.3
 d. IEC 3.2
 e. IEC 3.9
 f. AU 3.3
 g. ISC 3.0
 h. CMU 3.15
 i. CLK 3.0
 j. IEC 3.7
5. a. ISC 3.3
 b. 20-23, 25-27, and 43
6. a. Page 12
 b. Coordinate 43C6
7. IEC 3.10
8. a. Figure A-13
 b. ISC 3.7
 c. Pages 111 through 119

LEARNING ACTIVITY 2-C. REFERENCE READING: CPU CLOCK

This activity describes the theory of operation for the CPU clock.

OBJECTIVES

- You will be able to state the characteristics of the clock in the CPU.
- You will be able to follow the clock distribution logic in the CPU.

Directions: Locate DPD CLK 3.0 and the theory of operation description on page 156.48, found in the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual, publication number 60456170.

Read the theory of operation and reference it to the logic on CLK 3.0.

In the logic, pay particular attention to the waveforms drawn in the VA and TX paks. Note that T5 is a 50 nanosecond clock generated from phases 1 and 3. Also note that T6 is a 50 nanosecond clock generated from phases 2 and 4. T5 is the clock most commonly used in the CPU.

When you have finished studying the clock diagrams, you may proceed to your next assigned activity.

CYBER 170 Model 720/730 CPU
Learning Activity 2-D

**LEARNING ACTIVITY 2-D. REFERENCE READING:
IEC 3.0 THEORY OF OPERATION**

This activity describes the theory of operation for IEC 3.0.

OBJECTIVES

- You will be able to follow the paths on input data into the CPU from CMC in the DPDs.
- You will be able to locate CPU input control signals in the DPDs.

Directions: Locate DPD IEC 3.0 and the theory of operation description in the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual, publication number 60456170.

In this student manual, locate the CPU block diagram, figure 1-5. Note the CR9 input register in the upper left. The diagrams in IEC 3.0 is the logic for CPU input from CMC.

Now read the theory of operation for IEC 3.0 in the manual. Read the theory of operation and relate its content to the logic diagrams. If you wish to make notes on the diagrams, feel free to do so.

When you have completed your reading, you may continue to your next assigned activity.

LEARNING ACTIVITY 2-E. EXERCISE: IEC 3.0 THEORY OF OPERATION REVIEW

This activity reinforces what you learned about CPU inputs in learning activity 2-D.

OBJECTIVES

- You will be able to follow the paths of input data into the CPU from CMC in the DPDs.
- You will be able to locate CPU input control signals in the DPDs.

Directions: The following questions refer to IEC 3-0 in the CPU diagrams. Answer the following questions by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of each activity.

- What are the pak types that contain register CR9 in CPU-0? VJ
 - What are the pak types that contain register CSUD in CPU-1? KR
- What is chassis location of the pak which contains bit 20 of CR9 in CPU-0? 1N20
- Some of the CPU-0 CR9 bits go through fan-outs on IEC 3.0. Which bits are they? 36-59
- How often is register CR9 clocked (loaded)? 75-50 NSEC
- In CPU-1 what is the chassis location of the pak that contains bit 42 of the CSUD register? 4N10
 - What other paks on IEC 3.0 does bit 42 go through? 4N15 and 4N16
- The Master Clear signal comes into the CPU to a KR pak type located at 1Q07.
- The Request Exchange signal comes into CPU-1 to a KR pak type located at 4N13.

This completes the exercise on IEC 3.0 logic. If you wish you may review this activity before proceeding to your next activity.

CYBER 170 Model 720/730 CPU
Learning Activity 2-E

ANSWERS FOR LEARNING ACTIVITY 2-E

1. a. VJ
 b. KR
2. 1N20 Remember CPU-0 is in chassis 1.
3. Bits 36-59. These bits feed more circuits than bits 0-35.
 Therefore they need to go through the fan-outs.
4. CR9 is loaded every 50 nanoseconds by clock T5.
5. a. 4N10. CPU-1 is in chassis 4
 b. VC paks at 4N15 and 4M16
6. KR, Q07
7. KR, 4N13

**LEARNING ACTIVITY 2-F. REFERENCE READING:
IEC 3.1 THEORY OF OPERATION**

OBJECTIVES

- You will be able to state the functions of the logic on IEC 3.1, instruction word disassembly and function decode.
- You will be able to follow instruction data through the U1, U2, U3, and RNI Hold registers.

Directions: Locate IEC 3.1 and the theory of operation description for the U1, U2, U3 and RNI Hold registers found in the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual, publication number 60456170.

Read the theory of operation description for the U1, U2, U3 and the RNI Hold registers while referencing IEC 3.1 and figure 1-5 in this student manual.

When you are satisfied with your understanding of the material, you may proceed to your next assigned activity.

CYBER 170 Model 720/730 CPU
Learning Activity 2-G

LEARNING ACTIVITY 2-G. EXERCISE:
IEC 3.1 THEORY OF OPERATION REVIEW

This activity reinforces what you learned about IEC 3.1 in learning activity 2-F.

OBJECTIVES

- You will be able to state the function of the logic on IEC 3.1, instruction word disassembly and function decode.
- You will be able to follow instruction data through the U1, U2, U3, and RNI Hold registers.

Directions: Answer the following questions about the logic on page IEC 3.1 by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of this activity.

1. How many bits are in each of the following registers?
 - a. U1 60
 - b. U3 15
 - c. RNI Hold 30
2. Each FU type pak contains 2 bits of U3.
3. What is the chassis location of the pak that contains each of the following.
 - a. U3, bit 8 H01
 - b. U1, bit 40 H02
 - c. RNI RGTR, bit 15 G01
4. The signals that control what is gated through U2 are called PC0 and PC1. These signals are generated by the count in the PARCEL COUNTER.
5. If the parcel counter count equals 2, which parcel is gated through U2? PARCEL 2
6. The content of U3 is visually displayed in the CPU chassis on a BZ type pak located at G05.
7. What is the purpose of the FK pak located at G07? FUNCTION DECODE

CYBER 170 Model 720/730 CPU
Learning Activity 2-G

8. The content of U3 is 36123. Which of the following outputs of the function decode (FK @ G07) are active? _____
- a. FEQ010
 - ☒ b. FMEQ36
 - ☒ c. FM3637
 - d. FUNEQ6
9. The inputs to U1 come from register CR9 U1 is loaded by clock T5 if the signal ENVI is present.
10. The output path from U2 that leaves the FU paks before entering U3 is used when the CPU is executing a 30 bit instruction.

This concludes the exercise on the instruction registers. When you are ready, you may proceed to your next assigned activity.

CYBER 170 Model 720/730 CPU
Learning Activity 2-G

ANSWERS FOR LEARNING ACTIVITY 2-G

1. a. 60
 b. 15
 c. 30
2. 2 bits
3. a. H01
 b. H02
 c. G01
4. PC0, PC1; parcel counter
5. Parcel 2
6. BZ, G05
7. It does decoding of the content of U3 bits 6-14. These bits correspond to the f, m, and i portions of the CPU instruction.
8. b and c
9. CR9; ENU1 (Enable U1)
10. 30 bit instruction. These are the K bits of the instruction.

**LEARNING ACTIVITY 2-H. REFERENCE READING:
IEC 3.2 THEORY OF OPERATION**

This activity describes the theory of operation for IEC 3.2.

OBJECTIVE

- You will be able to trace data paths through the CPU's X, A, and B operating registers.

Directions: Locate IEC 3.2 and the theory of operation description for the X, A, and B operating registers found in the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual, publication number 60456170.

Read the theory of operation description for the X, A, and B registers while referencing IEC 3.2 and figure 1-5 in this student manual.

When you are satisfied with your understanding of the material, you may proceed to learning activity 2-I.

CYBER 170 Model 720/730 CPU
Learning Activity 2-I

LEARNING ACTIVITY 2-I. EXERCISE:
IEC 3.2 THEORY OF OPERATION REVIEW

This activity reinforces what you learned about IEC 3.2 in learning activity 2-H.

OBJECTIVE

- You will be able trace data paths through the CPU's X, A, and B operating registers.

Directions: Answer the following questions about the logic for the X, A, and B registers on IEC 3.2 by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of this activity.

1. The X, A, and B registers are contained in 42 type of paks. Each pak contains 6 bits of 8 registers.
2. What is the pak location for each of the following?
 - a. X bit 21 G12
 - b. A bit 3 102
 - c. B bit 14 209
3. An X register can be selected by using the I, J, or K designator of the instruction.
4. Locate each of the following signals on IEC 3.2 and list the pak type and location where each is generated.
 - a. SELXK GC @ H08
 - b. NSELXI GC @ H08
 - c. AX1-3 XT @ G08
 - d. ENABX GC @ H08
 - e. AA1-3 YH @ I01
 - f. AB1-3 XH @ I06
5. The inputs to the X registers come from I02 047 or from CR9. The input to be used is determined by the signal CR9X.
6. Reference the YG pak at I21. Answer the following questions:
 - a. What is its input? X47-59
 - b. When is the signal EXP01 generated? X48-59=0000
 - c. The signal X59N47 is generated if: X59-47

CYBER 170 Model 720/730 CPU
Learning Activity 2-I

7. The inputs to the A registers come from F017 and CR9 18-23
8. B register inputs are from F017 and CR9.017
9. Reference the YH pak at I06. When is the signal BLKB generated? What is its function? when selected Block RD output

This completes the exercise on X, A, and B register logic. You may proceed to the next activity in your assignment.

CYBER 170 Model 720/730 CPU
Learning Activity 2-I

ANSWERS FOR LEARNING ACTIVITY 2-I

1. UZ; 6 bits; 8 registers
2.
 - a. G12
 - b. I02
 - c. I09
3. i, j, or k
4.
 - a. GC @ H08
 - b. GC @ H08
 - c. YH @ G08
 - d. GC @ H08
 - e. YH @ I01
 - f. YH @ I06
5. CR9 or c bits 96-105 and I52 bits 0-47; gated by signal CR9X
6.
 - a. X bits 47-59 (exponent bits)
 - b. If bits 48-59 of X are 0000 or 7777 (exponent is zero)
 - c. Bit 47 is not equal to bit 59. This is used to determine if a floating point operand is normalized.
7. CR9 or F register
8. CR9 or F register
9. Whenever register B0 is addressed. It causes the output of B0 to be blocked on the UZ paks. This forces B0 to zero at all times. There is a B0 register physically present in the CPU. Its output is always blocked.

**LEARNING ACTIVITY 2-J. REFERENCE READING:
IEC 3.3 AND 3.4 THEORY OF OPERATION**

This activity describes the theory of operation for IEC 3.3 and 3.4.

OBJECTIVES

- You will be able to trace the data paths and control signals for the P, RAC, FLC, and MA CPU control registers.
- You will be able to trace data paths and control signals through the EM/EE control registers.

Directions: Locate IEC 3.3 and IEC 3.4 and the theory of operation description for the P, RAC, FLC, MA, and the EM/EE registers found in the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual, publication number 60456170.

Read the theory of operation description for these registers while referencing IEC 3.3 and IEC 3.4 as well as figure 1-5 in this student manual. The K1 and K2 registers will be covered in greater detail as part of the compare/move unit module.

When you are satisfied with your understanding of the material, you may proceed to learning activity 2-K.

LEARNING ACTIVITY 2-K. EXERCISE:
IEC 3.3 AND 3.4 THEORY OF OPERATION REVIEW

This activity reinforces what you learned about IEC 3.3 and 3.4 in learning activity 2-J.

OBJECTIVES

- You will be able to trace the data paths and control signals for P, RAC, FLC, and MA registers.
- You will be able to trace data paths and control signals through the EM/EE control registers.

Directions: Answer the following questions about the logic found on IEC 3.3 and 3.4 by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of the activity.

1. The P, RAC, MA, and FLC registers are located on FP type paks. Each pak contains 2 bit of each of the four registers.
2. What is the pak location of P register bit 10? J08.
3. The inputs to RAC, FLC, and MA come from CR9.
4. the P register has inputs from F and CR9.
5. The IO selector on the FP paks has inputs from 6 different registers. Which register is gated through IO is determined by the count in the three select code signals which are called S100, S101, and S102.
6. What select code will gate MA through IO? S102.
7. The IO select code is generated on the G-C type pack located at J14.
8. The content of the P register can be visually checked in the CPU chassis by reading the display module in location K23.
9. Reference IEC 3.4. The EM/EE registers are contained in a FW type pak at location J18.
10. The inputs to the EM register come from CR9.

CYBER 170 Model 720/730 CPU
Learning Activity 2-K

11. The EE register inputs come from error detection
circuits.
12. The EM/EE select circuit is controlled by a signal called EX214. If the signal is active, EM is gated through EM/EE Select. If the signal is inactive, EE is gated.
13. The output signal from J18 called ECONDS (error condition sensed) is generated when both bits are true
EE = 1 or EM = 1.

CYBER 170 Model 720/730 CPU
Learning Activity 2-K

ANSWERS FOR LEARNING ACTIVITY 2-K

1. FP; 2
2. J08
3. CR9 - These registers are loaded only during an exchange jump.
4. CR9 and F-P is loaded during an exchange jump. But it also is loaded with P+1 or a jump address which is formed in the small adder.
5. 6; SI00, SI01, and SI02
6. 2
7. GC @ J14
8. K23
9. FW @ J18
10. CR9 - EM is loaded only at exchange jump time.
11. The various sections in the CPU that can detect that an error has occurred.
12. IEX214 (an exchange jump timing signal); EM; EE
13. A bit in the EE register is set and its corresponding bit in the EM register was also set.

POST TEST

When you have completed the learning activities assigned for module 2, sign on to the PLATO terminal and take the module 2 test.

Depending on the results of the test, you will be told to either review some of the previous activities, or to go on to module 3.

MODULE 3

ARITHMETIC UNIT (AU) LOGIC

During this module you learn to follow data paths and control signals through the logic diagrams included in the AU section of the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual. The AU section includes the logic for both the large arithmetic section and the small arithmetic section.

PRETEST

To start this module, sign on to the PLATO terminal and read the objectives of this module. If you feel that you might be able to meet some of the objectives, take the module test. After evaluating the results of your test, PLATO Learning Management (PLM) will then assign the learning activities that relate to the objectives you did not meet. If you do not wish to take the test first, ask for an assignment.

LEARNING ACTIVITIES

In the "Assigned" column below, put a check mark by each activity assigned to you by PLM, then proceed through your assigned activities. Check off each activity as you complete it. You may choose to do all of these activities or do some activities more than once.

<u>Assigned</u>	<u>Completed</u>	<u>Activity</u>	<u>Description</u>	<u>Page</u>
_____	_____	3-A	Reference Reading: AU 3.3 Theory of Operation. This learning activity covers the theory of operation of AU 3.3.	3-5
_____	_____	3-B	Exercise: AU 3.3 Theory of Operation Review. This learning activity reinforces what you learned about AU 3.3.	3-6

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Module 3

<u>Assigned</u>	<u>Completed</u>	<u>Activity</u>	<u>Description</u>	<u>Page</u>
_____	_____	3-C	Reference Reading: AU 3.2 Theory of Operation. This learning activity covers the theory of operation of AU 3.2.	3-9
_____	_____	3-D	Exercise: AU 3.2 Theory of Operation Review. This learning activity reinforces what you learned about AU 3.2.	3-10
_____	_____	3-E	Reference Reading: AU 3.0 and 3.1 Theory of Operation. This learning activity covers the theory of operation of AU 3.0 and 3.1.	3-13
_____	_____	3-F	Exercise: AU 3.0 and 3.1 Theory of Operation Review. This learning activity reinforces what you learned about AU 3.0 and 3.1.	3-14
_____	_____	3-G	Reference Reading: AU 3.4 Theory of Operation. This learning activity covers the theory of operation of AU 3.4.	3-17
_____	_____	3-H	Exercise: AU 3.4 Theory of Operation Review. This learning activity reinforces what you learned about AU 3.4.	3-18
_____	_____	3-I	Reference Reading: AU 3.5 and 3.6 Theory of Operation. This learning activity covers the theory of operation of AU 3.5 and 3.6.	3-20
_____	_____	3-J	Exercise: AU 3.5 and 3.6 Theory of Operation Review. This learning activity reinforces what you learned about the theory of operation of AU 3.5 and 3.6.	3-21

CYBER 170 Model 720/730 CPU
Module 3

<u>Assigned</u>	<u>Completed</u>	<u>Activity</u>	<u>Description</u>	<u>Page</u>
_____	_____	3-K	Reference Reading: AU 3.7 and 3.8 Theory of Operation. This learning activity covers the theory of operation of AU 3.7 and 3.8.	3-25
_____	_____	3-L	Exercise: AU 3.7 and 3.8 Theory of Operation Review. This learning activity reinforces what you learned about AU 3.7 and 3.8.	3-26

CYBER 170 Model 720/730 CPU
Module 3

**LEARNING ACTIVITY 3-A. REFERENCE READING:
AU 3.3 THEORY OF OPERATION**

This activity describes the theory of operation for AU 3.3.

OBJECTIVE

- You will be able to follow data paths and identify control signals for the I5, C, and I15 registers in logic diagrams on page AU 3.3 in the CPU diagrams manual.

Directions: Review the large arithmetic section in the CPU detailed block diagram, figure 1-5, before you start reading the theory of operation. Make sure you can identify all I5 inputs and C register outputs on the block diagram. Also note I15 input and output paths.

Locate DPD page AU 3.3 in your Hardware Maintenance Manual, publication number 60456170. Become familiar with the content of this logic page.

Refer to the AU 3.3 and read its theory of operation in the theory of operation section of the Hardware Maintenance Manual.

When you have finished studying AU 3.3 logic, you may proceed to your next assigned activity.

LEARNING ACTIVITY 3-B. EXERCISE: AU 3.3 THEORY OF OPERATION REVIEW

This activity reinforces what you learned about AU 3.3 in learning activity 3-A.

OBJECTIVE

- You will be able to follow data paths and identify control signals for the I5, C, and I15 registers in logic diagrams on page AU 3.3 in the CPU diagrams manual.

Directions: Refer to the AU 3.3 logic and its theory of operation. Answer the following questions by writing the most appropriate word or words in each blank. You may also reference the CPU detailed block diagram, figure 1-5 in this student manual.

- The I5, I5 complement control, and C registers are contained in FC type paks. Each pak contains 3 bits of each register.
- The I15 register is contained on _____ type paks. Each pak contains _____ bits of I15.
- Give the chassis location of each of the following register bit positions.
 - C register, bit 19 E36
 - I5 register, bit 97 D28
 - I15 register, bit 45 E14
- I5 is controlled by a 3 bit select code which determines which one of 8 (number) inputs is gated through it.
- For each I5 select code value listed below, enter the input that is gated through it to the C register.

<u>I5 Select Code</u>	<u>Input Enabled</u>
a. 0	<u>LOGICAL 05</u>
b. 1	<u>DJ</u>
c. 2	<u>C</u>
d. 3	<u>LOGICAL 45</u>
e. 4	<u>I45</u>
f. 5	<u>RK-3</u>
g. 6	<u>zero fill</u>
h. 7	<u>logical 65</u>

6. The I5 Complement Control register is controlled by the I5C--signals generated on the GX type pak located at F23.
7. Reference the GX pak at F23. Which I5 complement bits are controlled by each output signal from the GX pak?
 - a. I5C06 0-46
 - b. I5C232 47
 - c. I5C85 48-65 66-95
 - d. I5C67 96-107
8. Which pak controls when the C register is to be enabled for loading? GC at H26.
9.
 - a. F register, bits 0-17, go to I15 bits 0-17 at pak locations E07, E08, and E09.
 - b. F register, bits 0-11, also go to I15 bits 48-59 at pak locations E15, E16, and _____.
10. I15 bit 30 inputs to I5 bit 78 at pak location D35.

This completes the exercise on AU 3.3 logic. After you check your answers, you may proceed to your next assigned activity.

CYBER 170 Model 720/730 CPU
Learning Activity 3-B

ANSWERS FOR LEARNING ACTIVITY 3-B EXERCISE

1. FC paks; 3 bits
2. JA paks; 6 bits
3. a. E36
b. D28
c. E14
4. 3; 8
5. a. 0 = Logical zeros (0)
b. 1 = D register
c. 2 = C register
d. 3 = Logical fours (4g)
e. 4 = I45 to bits 0-6, zeros to bits 7-47, and I15 to bits 48-107.
f. 5 = Shift network, rank 3
g. 6 = Zeros to bits 0-47, and X register to bits 48-107
h. 7 = Logical sixes (6g)
6. GX at F23
7. a. Bits 0-46
b. Bit 47
c. Bits 48-95
d. Bits 96-107
8. GC at H26
9. a. I15 bits -17 at E07, E08, and E09
b. I15 bits 48-59 at E15 and E16
10. Bit 78 at D35 (I15 bits 0-59 feed I5 bits 48-107)

**LEARNING ACTIVITY 3-C. REFERENCE READING:
AU 3.2 THEORY OF OPERATION**

This activity describes the theory of operation for AU 3.2.

OBJECTIVE

- You will be able to identify the signals which generate the I5 select code and state which I5 bits are controlled by each signal.

Directions: Locate DPD page AU 3.2 in your Hardware Maintenance Manual, publication number 60456170. Become familiar with the contents of this logic page.

Refer to the AU 3.2 and read its theory of operation in the theory of operation section of the Hardware Maintenance Manual.

When you are ready, you may proceed to your next assigned activity.

CYBER 170 Model 720/730 CPU
Learning Activity 3-D

LEARNING ACTIVITY 3-D. EXERCISE:
AU 3.2 THEORY OF OPERATION REVIEW

This activity reinforces what you learned about AU 3.2 in learning activity 3-C.

OBJECTIVE

- You will be able to identify the signals which generate the I5 select code and state which I5 bits are controlled by each signal.

Directions: Answer the following questions about the logic on AU 3.2 by writing the most appropriate word or words in each blank. You may also refer to the theory of operation for AU 3.2.

Compare your answers with those given at the end of this activity.

- The generation of bit 0 (2⁰) of the I5 select code is controlled by the logic in the GX paks at locations F21, F20, and F19.
- The generation of bit 1 (2¹) of the I5 select code is controlled by the logic in the GX paks at locations F20, F22, and F21.
- I5 select code bit 2 (2²) generation is controlled by the logic in the GX paks at locations F19, F22, and F21.
- The I5 select code bit 0 signal which controls bits 0-44 of I5 is generated on the GX pak at F19 and goes through the fan-out pak at location H36.
- What three signals are the I5 select code bits for I5 bits 105-107? I5S136 I5S236 I5S436
- For each of the following signals, list the I5 bits it controls and the location of the pak from which the signal leaves AU 3.2.

Signal Name	I5 Bits	Pak Location
a. I5285	48-71 78-95	<u>F21</u>
b. I5104	<u>0-44</u>	<u>H36</u>
c. I5208	<u>0-8</u>	<u>F34</u>
d. I5S116	<u>45-47</u>	<u>F20</u>
e. I5S13	<u>96-104</u>	<u>F07</u>
f. I5164	<u>96-104</u>	<u>F34</u>

CYBER 170 Model 720/730 CPU
Learning Activity 3-D

This completes the exercise. After checking your answers, you may proceed to your next assigned activity.

CYBER 170 Model 720/730 CPU
Learning Activity 3-D

ANSWERS FOR LEARNING ACTIVITY 3-D

1. F21, F20, and F19
2. F20, F22, and F21
3. F19 and F22
4. F19; H36
5. I5S136
I5S236
I5S436
6.

a.	48-71, 78-95	E21
b.	0-44	H36
c.	0-8	I34
d.	45-47	F20
e.	96-104	F07
f.	96-104	I34

**LEARNING ACTIVITY 3-E. REFERENCE READING:
AU 3.0 AND 3.1 THEORY OF OPERATION**

This activity describes the theory of operation for AU 3.0 and 3.1.

OBJECTIVE

- You will be able to follow data paths and locate control signals for the I14, I4, and D registers and through the D adder (large adder) in the logic diagrams on pages AU 3.0 and 3.1.

Directions: Review the large arithmetic section in the CPU Detailed Block Diagram, figure 1-5, before you start reading the theory of operation. Make sure you can follow data paths on the block diagram. Note all input and output paths to the D adder and D register.

Locate DPD pages AU 3.0 and AU 3.1 in your Hardware Maintenance Manual, publication number 60456170. Become familiar with the contents of these pages.

Refer to AU 3.0 and AU 3.1 and read the theory of operation in the theory of operation section of the Hardware Maintenance Manual.

When you have finished studying the logic on these two pages, you may proceed to the next assigned activity.

LEARNING ACTIVITY 3-F. EXERCISE:
AU 3.0 AND 3.1 THEORY OF OPERATION REVIEW

This activity reinforces what you learned about AU 3.0 and 3.1 in learning activity 3-E.

OBJECTIVE

- You will be able to follow data paths and locate control signals for the I14, I4, and D registers and through the D adder in the logic diagrams in pages AU 3.0 and AU 3.1.

Directions: Refer to the AU 3.0 and 3.1 and their theory of operation descriptions, answer the following questions by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of this activity.

1. The D register is contained in FD type paks, and each pak contains 4 bits of the D register.
2. Reference the D adder logic unit. What is the input to the adder's A input; B input and C input?
 - a. A input = D
 - b. B input = C
 - c. C input = CARRY
3. What is the pak location of D register bit 73? F35
4. I4 can perform four different functions. What are these four functions?
Zero fill
Right shift
Left shift
no shift
5. The two signals that control the function of I4 are I40 and I41.
6.
 - a. I14 has inputs from D and D ADDER.
 - b. The signal that selects which input is gated through I14 is called I14 S and it is generated on pak at location G30.
7. The control for when the D register is enabled (loaded) is performed on the GC pak at location H26.

CYBER 170 Model 720/730 CPU
Learning Activity 3-F

8. What is the function of the signals DAS0, DAS2, DAS3, and DA-M that feed the ALU circuit? Address Function Codes
9. Reference AU 3.1. The first state carry look-ahead pak for bits 64-79 is located at F33.
10. The second state carry look-ahead pak for bits 48-107 is located at G30.
11. The signal CN8891 is generated on the pak at location F32, and it feeds the D ALU circuit pak located at F28.

This completes the exercise on AU 3.0 and 3.1 logic. After you have checked your answers, you may proceed to your next assigned activity.

CYBER 170 Model 720/730 CPU
Learning Activity 3-F

ANSWERS FOR LEARNING ACTIVITY 3-F

1. FD: 4 bits
2.
 - a. D register
 - b. C register
 - c. Carry inputs from the carry function circuits (AU 3.1)
3. F35
4. Generate all zeroes input to D.
Right shift its input by one place.
Left shift its input by one place.
Pass its input straight through.
5. I40 and I41
6.
 - a. D register and D ALU
 - b. I14S; G30
7. H26
8. They are the D adder function code that determine the type of operation performed in the ALU chip (Add, Exclusive OR, Logical Product, and so forth).
9. F33
10. G30
11. F32; F28

**LEARNING ACTIVITY 3-G. REFERENCE READING:
AU 3.4 THEORY OF OPERATION**

This activity describes the theory of operation of AU 3.4.

OBJECTIVE

- You will be able to follow data paths and locate control signals for registers I9, I19, and the shift counter in logic diagrams on page AU 3.4.

Directions: Review the operation, inputs, and outputs, of I19, I9, and the SK Counter on the CPU detailed block diagram, figure I-5.

Locate AU 3.4 in your Hardware Maintenance Manual, publication number 60456170.

Refer to the AU 3.4 logic and read its theory of operation in the theory of operation section of the Hardware Maintenance Manual.

When you have completed your study of AU 3.4 logic, you may proceed to the next activity.

LEARNING ACTIVITY 3-H. EXERCISE:
AU 3.4 THEORY OF OPERATION REVIEW

This activity reinforces what you learned about AU 3.4 in learning activity 3-G.

OBJECTIVE

- You will be able to follow data paths and locate control signals for registers I9, I19, and the shift counter in logic diagrams on page AU 3.4.

Directions: Refer to the AU 3.4 and its theory of operation, answer the following questions by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of this activity.

1. The shift counter and I9 are located on FS type paks at locations C24 and C23.
2. I19 is located on JK type paks at locations E01 through E06.
3. The function of the SK CNTR is determined by signals SKS1 and SKS2 which originate on the GC pak at location F26.
4. I19 normally gates U3 bits 0-5 to I9 unless a COMPARE / MOVE instruction is being executed.
5. What two preselected constants can be generated in I9?
111100 110000

This completes the exercise on AU 3.4 logic. When you have checked your answers you may proceed to your next assigned activity.

ANSWERS FOR LEARNING ACTIVITY 3-H

1. FS; C23 and C24
2. JK; EO1 through EO6
3. SKS1 and SLS2; I26
4. 0-5; compare/move
5. 74g and 60g

CYBER 170 Model 720/730 CPU
Learning Activity 3-I

**LEARNING ACTIVITY 3-I. REFERENCE READING:
AU 3.5 AND 3.6 THEORY OF OPERATION**

This activity describes the theory of operation for AU 3.5 and 3.6.

OBJECTIVE

- You will be able to follow data paths and locate control signals in the shift network and the normalize network logic diagrams on pages AU 3.5 and 3.6 of the CPU manual.

Directions: Review the shift network and normalize network inputs and outputs on the CPU detailed block diagram, figure 1-5.

Locate DPD pages AU 3.5 and 3.6 in the Hardware Maintenance Manual, publication 60456170. Briefly examine the content of these two logic pages before reading the theory of operation.

Refer to the AU 3.5 and 3.6 and read their theory of operation descriptions in the Theory of Operation section of the Hardware Maintenance Manual.

When you are ready to go on, you may proceed to the next activity in your assignment.

LEARNING ACTIVITY 3-J. EXERCISE:
AU 3.5 AND 3.6 THEORY OF OPERATION REVIEW

This activity reinforces what you learned about AU 3.5 and AU 3.6 in learning activity 3-I.

OBJECTIVE

- You will be able to follow data paths and locate control signals in the shift network and the normalize network logic diagrams on pages AU 3.5 and 3.6 of the CPU manual.

Directions: Refer to the DPDs and AU 3.5 and 3.6 and their theory of operation descriptions. Answer the following questions by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of this activity.

1. Shift network rank 1 logic circuits are contained on U15 type paks, and they are located in chassis positions B 25 through B 32 and C 45 through C 31.
2. The data input to SN rank 1 is from the C register. The input lines are labeled CS# 0-107.
3. SN rank 1 output data signals are labeled 182-0107.
4. Which bits of the shift counter control the amount of shifting done in rank 1? SK 3-5
5. SN rank 1 can shift data 0, 8, 16, 24, 32, 40, 48, or 56 places to the right.
6. a. C register bit 85 comes into SN rank 1 at pak locations C30, C29 and B29.
b. If the shift count is equal to 30, input bit 85 to rank 1 will leave Rank 1 as bit 61 from pak location C29.
7. Reference AU 3.6. Rank 2 of the shift network is contained in U9 type paks located in chassis positions A27 through A40.
8. During a left shift operation, rank 2 performs a left shift of 3 places. During a right shift operation, rank 2 will right shift the data 0 or 64 places.

CYBER 170 Model 720/730 CPU
Learning Activity 3-J

9. Bit 55 from SN rank 1 comes into rank 2 at pak location A 34.
10. Rank 3 of the shift network is contained in UR type paks located in chassis positions B 33 through B 42 and C 38 through C 42.
11. Which bits of the shift counter control the amount of shifting in Rank 3? SKO-2
12. Rank 3 can shift data 0 to 7 places depending on the shift count.
13. Rank 3 output bit 105 leaves from the pak at location C38.
14. The output of rank 3 goes to C I5 and then into the register.
15. Reference AU 3.5. The normalize network is comprised of three US type paks and one FN type pak. The four paks are located at chassis positions C33 through C36.
16. The data input to the NN is from bits 48-95 of the C register.
17. The output of the NN is a 6-bit shift count that is the number of places a coefficient must be shifted to get its Most Significant Bit into bit 47 of a floating point operand.

This completes the exercise on the shift network and the normalize network. After you have checked your answers, you may proceed to your next assigned activity.

CYBER 170 Model 720/730 CPU
Learning Activity 3-J

The answers for this learning activity are on the following page.

CYBER 170 Model 720/730 CPU
Learning Activity 3-J

ANSWERS TO LEARNING ACTIVITY 3-J

1. UP paks; B25 through B32 and C25 - C32
2. C; CS1 0-107
3. 1S2 0-107 go to rank 2
1S2 0-47 go to the X registers
4. Bits 3-5 of the shift counter (SK 3-5)
5. 0, 8, 16, 24, 32, 40, 48, or 56 decimal places.
6. a. C29, C30 and B29
b. 61; C29-A shift count of 30_8 is equal to 24_{10} .
Rank 1 only shifts right so bit 85 must become bit 61 at the output.
7. UQ; A27-A40
8. 3; 0 of 64
9. A34
10. UR paks; B33-B42 and C38-C42
11. Bits 0-2 of the shift counter (SK0-2)
12. 0-7 places
13. C38
14. I5; C
15. US; FN; C33 - C36
16. Bits 48-95 of the C register
17. 6; most significant bit

**LEARNING ACTIVITY 3-K. REFERENCE READINGS:
AU 3.7 AND 3.8 THEORY OF OPERATION**

This activity describes the theory of operation for AU 3.7 and 3.8.

OBJECTIVE

- You will be able to follow data paths and locate control signals in the AU 3.7 and 3.8 logic diagrams for the small arithmetic section of the CPU.

Directions: Review the elements, inputs, and outputs of the small arithmetic section in the CPU detailed block diagram, figure 1-5.

Locate DPD's AU 3.7 and 3.8 in the Hardware Maintenance Manual, publication number 60456170. Briefly examine the contents of each page before reading the theory of operation.

While referencing AU 3.7 and 3.8, read their descriptions in the theory of operation section of the Hardware Maintenance Manual.

When you have finished studying these two pages you may proceed to the next activity.

CYBER 170 Model 720/730 CPU
Learning Activity 3-L

LEARNING ACTIVITY 3-L. EXERCISE:
AU 3.7 AND 3.8 THEORY OF OPERATION REVIEW

This activity reinforces what you learned about AU 3.7 and 3.8 in learning activity 3-K.

OBJECTIVE

- You will be able to follow data paths and locate control signals in the AU 3.7 and 3.8 logic diagrams for the small arithmetic section of the CPU.

Directions: Refer to the DPD's AU 3.7 and 3.8 and their theory of operation descriptions in the CPU manual. Answer the following questions by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of this activity.

1. Reference AU 3.7. I3 and I3 complement control are located on FY type paks in R row of the CPU logic chassis.
2. Each pak contains 2 bits of I3.
3. I3 bit 5 is located at R04.
4. The control signals that enable (select) inputs to I3 are generated in GC type paks at locations I14 and R08.
5. Which of the following signals will cause the output of I3 to be complemented? _____
 - a. FI39I3
 - b. COMBI3
 - c. COI0I3
 - d. FAMI3C
6. Reference AU 3.8. The F adder is located on FR type paks in chassis locations I15 through I19.
7. The FF paks contain 4 bits of the E, F, and I2 registers in addition to the adder itself.

8. List the inputs to A, B, and C input sections of the F adder.
- a. A = F
b. B = E
c. C = CARRY
9. The input to the E register is from I3.
10. The input to I2 is from either I3 or FADDER.
11. All outputs from the SAS come from the F register.
12. The function of the F adder ALU is controlled by the five signals labeled FAS 0-3 FAM.
13. The enable to clock the F register is generated on the VN type pak at location K15.
14. The E register clock enable is generated on the VN type pak at location L26.
15. What is the function of the FA pak at I20 and the FB pak at G31? CARRY
16. F register bit 9 is located on the pak at chassis location F17.

This completes the exercise on the SAS logic diagrams. When you have checked your answers, you may then proceed to your next activity.

CYBER 170 Model 720/730 CPU
Learning Activity 3-L

ANSWERS TO LEARNING ACTIVITY 3-L

1. FY; F
2. 2
3. F04
4. GC; I14 and F08
5. d. FAMI3C is one of the signals in the equation to generate the I3 complement signal SCOMI3 in the GC pak at F08.
6. FF; I15 - I19
7. 4; E, F, and I2
8. a. A = F register
b. B = E register
c. C = Carry inputs
9. I3
10. I3 or F adder ALU
11. F
12. FAS 0-3 and FAM
13. GC at H19
14. GC at H18
15. They provide first stage and second stage carry look-ahead function for the five paks in the F adder.
16. I17

POST TEST

When you have completed the learning activities assigned for module 3, sign on to the PLATO terminal and take the module 3 test.

Depending on the results of the test, you will be told to either review some of the previous activities, or to go on to module 4.

MODULE 4

RNI AND RELATED SEQUENCES

During this module you will learn to follow the control signals and data paths through the detailed pak diagrams (DPDs) in the instruction execution control (IEC) section of the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual, publication number 60456170. The portions covered in this module will be those associated with the exchange jump, read next instruction (RNI), common time, accept, and address out of range Sequences; also the I7 selector, parity generator and the Output register and transmitters.

PRETEST

To start this module, sign on to the PLATO terminal and read the objectives of this module. If you feel that you might be able to meet some of the objectives, take the module test. After evaluating the results of your test, PLATO Learning Management (PLM) will then assign the learning activities that relate to the objectives you did not meet. If you do not wish to take the test first, ask for an assignment.

LEARNING ACTIVITIES

In the "Assigned" column below, put a check mark by each activity assigned to you by PLM, then proceed through your assigned activities. Check off each activity as you complete it. You may choose to do all of these activities or do some activities more than once.

<u>Assigned</u>	<u>Completed</u>	<u>Activity</u>	<u>Description</u>	<u>Page</u>
_____	_____	4-A	Reference Reading: IEC 3.5, Theory of Operation, Exchange Jump Sequence. This learning activity covers the Theory of Operation for the exchange jump sequence.	4-5
_____	_____	4-B	Exercise: IEC 3.5, Exchange Jump Sequence Review. This learning activity reinforces what you learned about the exchange jump sequence.	4-6

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Module 4

<u>Assigned</u>	<u>Completed</u>	<u>Activity</u>	<u>Description</u>	<u>Page</u>
_____	_____	4-C	Reference Reading: IEC 3.6, Theory of Operation, Read Next Instruction Sequence. This learning activity covers the Theory of operation for the read next instruction sequence.	4-9
_____	_____	4-D	Exercise: IEC 3.6, Read Next Instruction Sequence Review.. This learning activity reinforces what you learned about the read next instruction sequence.	4-15
_____	_____	4-E	Reference Reading: IEC 3.7, Theory of Operation, Common Time Sequence. This learning activity covers the theory of operation for the common time sequence.	4-17
_____	_____	4-F	Exercise: IEC 3.7, Common Time Sequence Review. This learning activity reinforces what you learned about the common time sequence.	4-18
_____	_____	4-G	Reference Reading: IEC 3.8, Theory of Operation, Accept Sequence. This learning activity covers the theory of operation for the accept sequence.	4-21
_____	_____	4-H	Exercise: IEC 3.8, Accept Sequence Review. This learning activity reinforces what you learned about the accept sequence.	4-22
_____	_____	4-I	Reference Reading: IEC 3.9, Theory of Operation, Address Out of Range Sequence. This activity covers the theory of operation for the address out of range sequence.	4-25

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Module 4

<u>Assigned</u>	<u>Completed</u>	<u>Activity</u>	<u>Description</u>	<u>Page</u>
_____	_____	4-J	Exercise: IEC 3.9, Address Out of Range Sequence Review. This activity reinforces what you learned about the address out of range sequence.	4-26
_____	_____	4-K	Reference Reading: IEC 3.10, Theory of Operation, I7 Selector, Parity Generator and OutputRegister/transmitters. This activity covers the theory of operation for the I7 selector, parity, generator output register/transmitter.	4-29
_____	_____	4-L	Exercise: IEC 3.10, Theory of Operation, I7 Selector, Parity Generator and Output Register/transmitters Review. This activity reinforces what you learned about the I7 selector parity generator, output register/transmitters.	4-30

CYBER 170 Model 720/730 CPU
Module 4

**LEARNING ACTIVITY 4-A. REFERENCE READING:
IEC 3.5 THEORY OF OPERATION,
EXCHANGE JUMP SEQUENCE**

During this activity you will learn about the control signals and data flow associated with the exchange jump sequence.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data flow utilized in the exchange jump sequence using the detailed pak diagram (DPD) IEC 3.5

Directions: Locate the following detailed pak diagram (DPD), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual, publication number 60456170.

- DPD IEC 3.5
- Theory of operation description for the exchange jump sequence
- Instruction flow sequence chart for exchange jump

Also locate the exchange jump description found in the CYBER 170 Computer Systems Models 720, 730, 740, 750 and 760 Hardware Reference Manual, publication number 60456100. This is found in the central processor programming section.

Review the exchange jump description found in the central processor programming section of the Hardware Reference Manual. Then read the theory of operation for the exchange jump while referring to DPD IEC 3.5 and the instruction flow sequence chart for the exchange jump.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data flow for the exchange jump sequence, proceed to learning activity 4-B. In learning activity 4-B you will be answering questions designed to reinforce your ability to comprehend the logic associated with the exchange jump sequence.

LEARNING ACTIVITY 4-B. EXERCISE:
IEC 3.5 EXCHANGE JUMP SEQUENCE REVIEW

This activity reinforces what you learned about the exchange jump sequence in learning activity 4-A.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data flow utilized in the exchange jump sequence using the detailed pak diagram (DPD) IEC 3.5

Directions: The following questions refer to DPD IEC 3.5 and the theory of operation description for the Exchange Jump Sequence. Answer the following questions by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of this activity.

1. What module types contain the exchange jump timing chain?
GF
2. How many 60-bit computer words are associated with the exchange package? 16
3. At what location of the exchange package would the RAC be located? N+1
4. At what location of the exchange package would the A7 be located? N+8
5. Which bit positions in N+6 in the exchange package would contain the information for the MA? 253-255
6. What bit locations are associated with the RAE for an exchange package, ESM mode? ECS mode? 36-53 42-56
7. What bit locations are associated with the FLE for an exchange package, ESM mode? ECS mode? 36-59 42-59
8. Only the CPU can initiate an exchange jump. True or False?
FALSE
9. Which flip flop generates the signal that sends data in the X registers to central memory? XI7
10. On what module and location would the XI7 flip flop be located? GF-527

CYBER 170 Model 720/730 CPU
Learning Activity 4-B

The answers for this learning activity are on the following page.

CYBER 170 Model 720/730 CPU
Learning Activity 4-B

ANSWERS FOR LEARNING ACTIVITY 4-B

1. GF
2. 16
3. N+1
4. N+7
5. $2^{35}-2^{53}$
6. $2^{36}-2^{53}$; $2^{42}-2^{56}$
7. $2^{36}-2^{59}$; $2^{42}-2^{59}$
8. false
9. XI7 flip flop
10. GE @ J27

**LEARNING ACTIVITY 4-C. REFERENCE READING:
IEC 3.6 THEORY OF OPERATION,
READ NEXT INSTRUCTION SEQUENCE**

During this activity you will learn about the control signals and data flow associated with the read next instruction (RNI) sequence.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data flow necessary for the execution of the read next instruction (RNI) sequences shown on DPD IEC 3.6.

Directions: Locate the following detailed pak diagram (DPD), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual, publication number 60456170.

- DPD IEC 3.6
- Theory of operation description for the read next instruction (RNI) sequence
- Instruction flow sequence chart for the read next instruction (RNI)

Read the theory of operation for the read next instruction while referring to DPD ISC 3.6 and the instruction flow sequence chart for initial start RNI.

Refer also to figures 4-1 and 4-2 which are simplified versions of DPDs used during RNI. Also included in this activity is a timing chart (Figure 4-3) that depicts the initial start RNI with a subsequent full RNI and parcel RNIs. Confirm for yourself the sequential control signals and data flow for the three types of RNI (initial, full and parcel). You will find sequences for the various instructions effect the timing relationship and they are included in this chart, although they will be covered in detail in future learning activities.

When you feel comfortable with your ability to locate, identify and describe the control signals and data flow for the read next instruction sequence, proceed to learning activity 4-D. You will be answering questions designed to reinforce your ability to comprehend the logic associated with the read next instruction sequence.

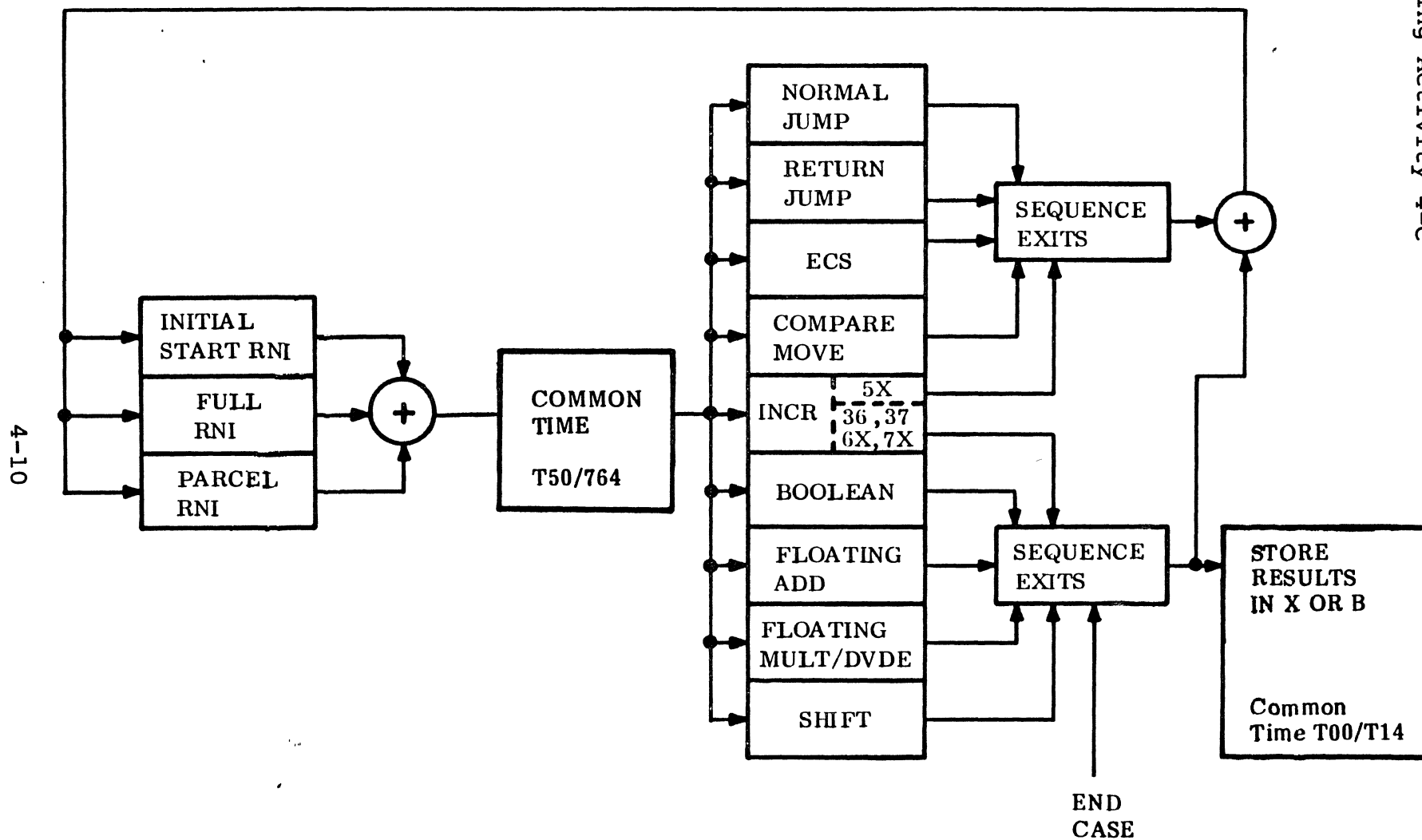


Figure 4-1. CYBER 170 Instruction Execution Block Flow

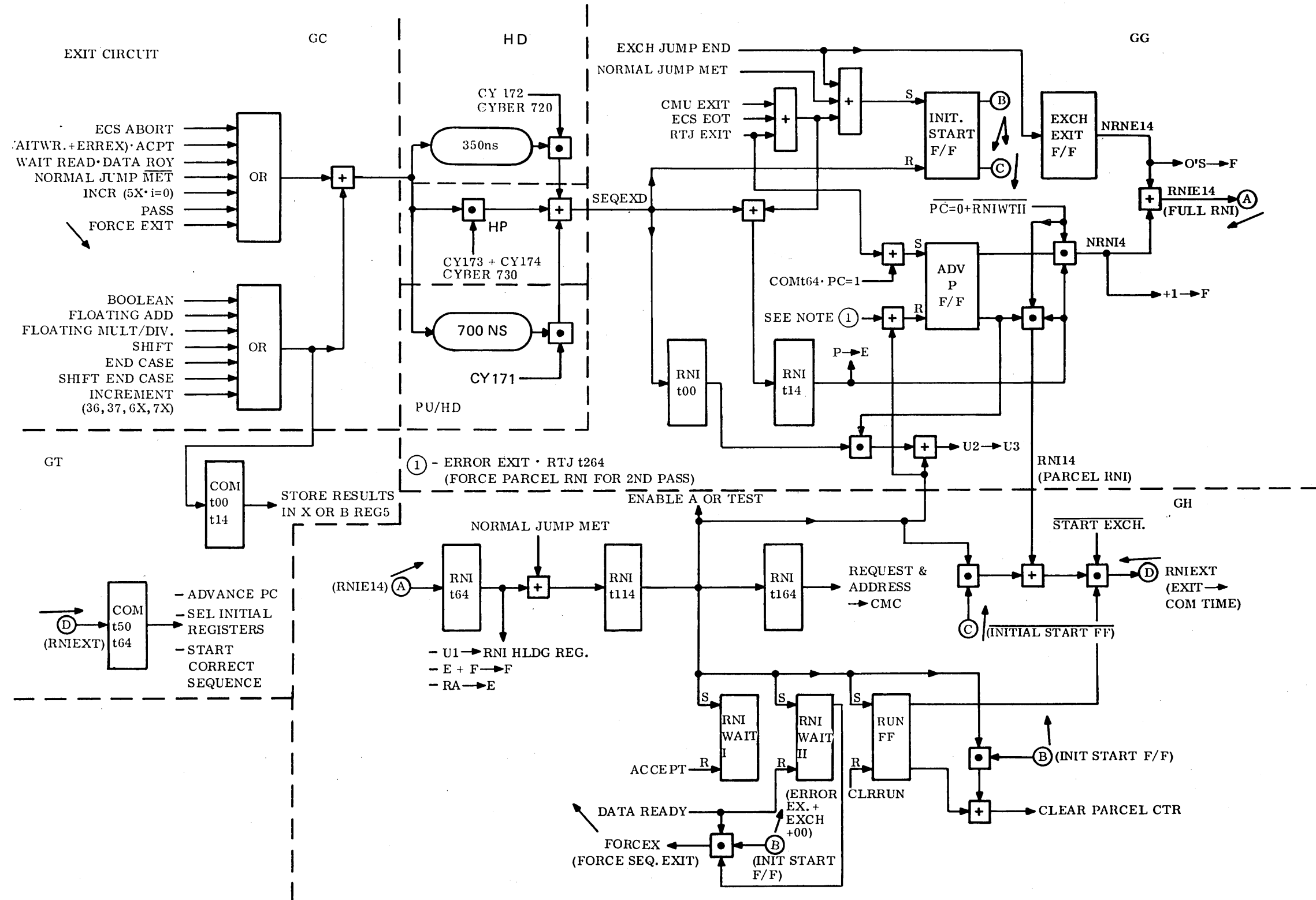


Figure 4-2. Simplified RNI Sequence Diagram

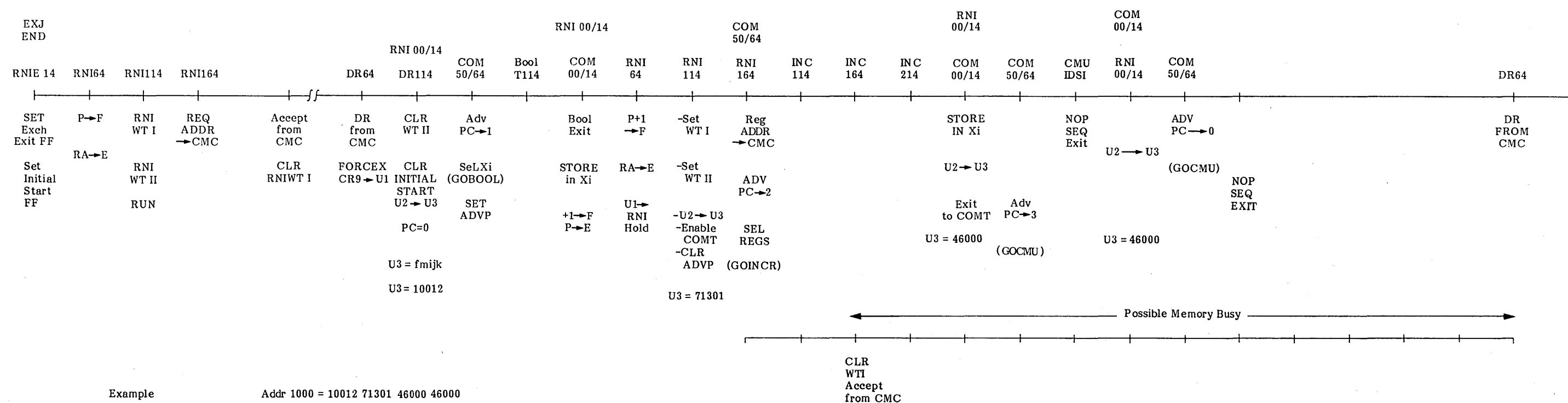


Figure 4-3. Typical RNI Timing Initial, Full, and Parcel

LEARNING ACTIVITY 4-D. EXERCISE: IEC 3.6 READ NEXT INSTRUCTION SEQUENCE REVIEW

This activity reinforces what you learned about the read next instruction sequence in learning activity 4-C.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data flow necessary for the execution of the read next instruction (RNI) sequences shown on DPD IEC 3.6.

Directions: The following questions refer to DPD IEC 3.6 and the theory of operation sequence. Answer the following questions by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of this activity.

- What are the three types of RNI? initial start RNI
full RNI, Parcel RNI
- What five signals can enable an initial start RNI?
MEX SEX
NJ DEXL
NRT JEX
NEAPDEX
EX JONE
- What is meant by an initial RNI? obtains a new
word from CM
- What is meant by a full RNI? normal RNI after
first instruction executed
- What is meant by a parcel RNI? word in seq exit
- On what module type and at what location is the initial start flipflop located? GA J2P
- On what module type and at what location is the RNI sequence timer that provides T64, T114 and T164? CH J2J
- What time is the PC counter cleared during initial start?
T114
- What is the length of the sequence exit delay? 350 nsec
- The count in the parcel counter is one count ahead of the parcel being executed. True or False? True

CYBER 170 Model 720/730 CPU
Learning Activity 4-D

ANSWERS FOR LEARNING ACTIVITY 4-D

1. Initial RNI
Full RNI
Parcel RNI
2. NECSEX - Normal ECS exit
NJPEXL - Normal jump condition met
NRTJEX - Return jump exit
NCMUEX - CMU exit
EXJONC, EXJRNI - Exchange jump exit
3. Obtaining a new 60-bit instruction word from CM
4. Obtains a new 60-bit instruction after execution of the first instruction of the word being processed.
5. It follows a sequence exit when advance P is absent, which indicates an additional parcel is available within the current instruction word.
6. GG @ J23
7. GH @ J22
8. T114
9. 350 ns
10. True

**LEARNING ACTIVITY 4-E. REFERENCE READING:
IEC 3.7 THEORY OF OPERATION,
COMMON TIME SEQUENCE**

During this learning activity, you will learn about the common time sequence.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data flow associated with the common time sequence as shown on DPD IEC 3.7.

Directions: Locate the following detailed pak diagram (DPD) and theory of operation description found in the CYBER 170 Models 720/730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPD IEC 3.7
- Theory of operation description for the common time sequence

Read the theory of operation for the common time sequence while referring to DPD IEC 3.7 for the common time sequence.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data flow for the common time sequence, proceed to learning activity 4-F. In learning activity 4-F you will be answering questions designed to reinforce your ability to comprehend the logic associated with the common time sequence.

LEARNING ACTIVITY 4-F. EXERCISE:
IEC 3.7 COMMON TIME SEQUENCE REVIEW

This activity reinforces what you learned about the common time sequence in learning activity 4-E.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data flow associated with the common time sequence as shown on DPD IEC 3.7.

Directions: The following questions refer to DPD IEC 3.7 and the theory of operation description for the common time sequence. Answer the following questions by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of this activity.

1. What is the module type and location of the module that provides COMT64, COMT50 signals? YD-H23
2. On what module is the ADVPC1 developed? YD H23
3. What is the module type(s) and location(s) of the module(s) that provides function decoding? GV-G22 GU-T22
4. What are the conditions necessary for a GOBOOL (Go Boolean) signal? F=1 @ COMT64

CYBER 170 Model 720/730 CPU
Learning Activity 4-F

The answers for this learning activity are on the following page.

CYBER 170 Model 720/730 CPU
Learning Activity 4-F

ANSWERS FOR LEARNING ACTIVITY 4-F

1. YD @ H23
2. YD @ H23
3. GU @ I22 and GV @ G22
4. GOBOOL : F = 1 . COMT64

**LEARNING ACTIVITY 4-G. REFERENCE READING:
IEC 3.8 THEORY OF OPERATION,
ACCEPT SEQUENCE**

During this learning activity you will learn about the Accept Sequence.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data flow associated with the accept sequence as shown on DPD IEC 3.8, and describe the relationship to RNI and read memory instructions.

Directions: Locate the following DPD and theory of operation description found in the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPD IEC 3.8
- Theory of operation description for the accept sequence

Read the theory of operation description for the accept sequence while referring to DPD IEC 3.8 for the accept sequence.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data flow for the accept sequence, proceed to learning activity 4-H. You will be answering questions designed to reinforce your ability to comprehend the logic associated with the accept sequence.

**LEARNING ACTIVITY 4-H. EXERCISE:
IEC 3.8 ACCEPT SEQUENCE REVIEW**

This activity reinforces what you learned about the accept sequence in learning activity 4-G.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data flow associated with the accept sequence as shown on DPD IEC 3.8, and describe the relationship to RNI and read memory instructions.

Directions: The following questions refer to DPD IEC 3.7 and the theory of operation description for the accept sequence. Answer the following questions by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of this activity.

1. What is the module type and location of the module that is labeled as the accept sequence timing CKT? YC-530
2. What signal enables the accept sequence timing chain? DT REDI
3. What happens when an address out of range fault occurs? NAR III starts accept sequence.
4. What is the purpose of the DRT 50 (YC pak) as a result of an increment read central memory reference? reads XI

CYBER 170 Model 720/730 CPU
Learning Activity 4-G

The answers for this learning activity are on the following page.

CYBER 170 Model 720/730 CPU
Learning Activity 4-G

ANSWERS FOR LEARNING ACTIVITY 4-H

1. YC @ J30
2. DTREDY
3. NARIIII from the address out of range sequence forces the start of a false accept sequence to force zeros into the CR9 register.
4. DRT 50 selects the Xi register to receive a data operand.

**LEARNING ACTIVITY 4-I. REFERENCE READING:
IEC 3.9 THEORY OF OPERATION,
ADDRESS OUT OF RANGE SEQUENCE**

During this activity you will learn about the address out of range (AOR) sequence.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data flow for the address out of range sequence as shown on DPD IEC 3.9.

Directions: Locate the following DPD and theory of operation description found in the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPD IEC 3.9
- Theory of operation description for the address out of range sequence

Read the theory of operation description for the address out of range sequence while referring to DPD IEC 3.9.

When you feel comfortable with your ability to locate, identify and describe the control signals and data flow for the address out of range sequence, proceed to learning activity 4-J. In learning activity 4-J you will be answering questions designed to reinforce your ability to comprehend the logic associated with the address out of range sequence.

LEARNING ACTIVITY 4-J. EXERCISE:
IEC 3.9 ADDRESS OUT OF RANGE SEQUENCE REVIEW

This activity reinforces what you have learned about the address out of range sequence in learning activity 4-I.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data flow for the address out of range sequence as shown on DPD IEC 3.9.

Directions: The following questions refer to DPD IEC 3.9 and the theory of operation description for the address out of range sequence. Answer the following questions by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of this activity.

1. What module type and at what location is the address out of range sequence timing count located? GL-J20
2. What module type and at what location is the address out of range test circuit located? PT-J19
3. What module type and at what location is the clear CR9 flip flop signal CLRR0? GL-J20
4. What conditions enable the enable memory request translator, GC @ K21? NRI-164 + NR264 + NIN264
+ EATOR
5. Name two signals that the error exit flip flop generates and describe the purpose of each one. ERRXT enables a return jump error exit sequence
CLR43 clears bit 3 instruction register

CYBER 170 Model 720/730 CPU
Learning Activity 4-J

The answers for this learning activity are on the following page.

CYBER 170 Model 720/730 CPU
Learning Activity 4-J

ANSWERS FOR LEARNING ACTIVITY 4-J

1. GL @ J20
2. FT @ J19
3. GL @ J20
4. NRI164 + NR264 + NIN264 + EATOR
5. EREXT enables a return jump error exit sequence
CLRU 3 clears the U3 Instruction register

**LEARNING ACTIVITY 4-K. REFERENCE READING:
IEC 3.10 THEORY OF OPERATION, I7 SELECTOR
PARITY GENERATOR, OUTPUT REGISTER/TRANSMITTER**

During this activity you will learn about the I7 selector, parity generator and the output register and transmitters.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data flow for the I7 selector, parity generator and the output register and transmitters, as shown on DPD IEC 3.10.

Directions: Locate the following DPD and theory of operation description found in the CYBER 170 Models 720/730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPD IEC 3.10
- Theory of operation description for the I7 selector, parity generator and the Output register and transmitters

Read the theory of operation description for the I7 selector, parity generator and the wutput register and transmitters while referring to DPD IEC 3.10.

When you feel comfortable with your ability to locate, identify and describe the control signals and data flow for the I7 selector, parity generator and the Output register and transmitters, proceed to learning activity 4-L. In learning activity 4-L you will be answering questions designed to reinforce your ability to comprehend the logic associated with the I7 selector, parity generator and the Output register and transmitters.

CYBER 170 Model 720/730 CPU
Learning Activity 4-L

LEARNING ACTIVITY 4-L. EXERCISE:
IEC 3.10 THEORY OF OPERATION, I7 SELECTOR,
PARITY GENERATOR, OUTPUT REGISTER/TRANSMITTER REVIEW

This activity reinforces what you learned about the I7 selector, parity generator, Output register and transmitters.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data flow for the I7 selector, parity generator and the Output register and transmitters, as shown on DPD IEC 3.9.

Directions: The following questions refer to DPD IEC 3.10 and the theory of operation description for the I7 selector, parity generator and the Output register and transmitters. Answer the following questions by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of this activity.

1. What module type and at what location would bit 59 be located for the I7 selector? FZ L24
2. Trace the bit 28 from the I7 selector to the output transmitter. FZ L04 RT-M02
3. At what location does bit 82 for the address/word count (IS2 60 through 82) enter the Output register? FZ Q18
4. What conditions the transfer of X being transferred to the HR register? CMT7 • CMX7
5. What signal indicates a CPU-0 data parity bit? At what module and location is it generated? KCPAR KC Q23
6. What signal clocks the contents of the HR register to the Output register? T5
7. What module and at what location generates is HR register bit 54? FZ L23

CYBER 170 Model 720/730 CPU
Learning Activity 4-K

The answers for this learning activity are on the following page.

CYBER 170 Model 720/730 CPU
Learning Activity 4-L

ANSWERS FOR LEARNING ACTIVITY 4-L

1. FZ @ L24
2. FZ @ L03 KT @ M02
3. EZ @ Q18
4. $\overline{\text{CM17}}$. CMX7
5. KCPAR (KC @ Q23)
6. T5
7. FZ @ L23

POST TEST

When you have completed the learning activities assigned for module 4, sign on to the PLATO terminal and take the module 4 test.

Depending on the results of the test, you will be told to either review some of the previous activities, or to go on to module 5.

MODULE 5

BOOLEAN AND INCREMENT SEQUENCES

During this module you will learn to follow control signals and data paths through the logic diagrams in the Instruction Sequence Control (ISC) section of the CYBER 170 Models 720, 730 CPU Hardware Maintenance Manual as described in the theory of operation section for the Boolean and increment instructions. The Boolean instructions covered will be the 10, 11, 12, 13, 14, 15, 16, 17 instructions and the increment instructions will be the 36, 37, 50-57, 60-67, and 70-77 instructions.

PRETEST

To start this module, sign on to the PLATO terminal and read the objectives of this module. If you feel that you might be able to meet some of the objectives, take the module test. After evaluating the results of your test, PLATO Learning Management (PLM) will then assign the learning activities that relate to the objectives you did not meet. If you do not wish to take the test first, ask for an assignment.

LEARNING ACTIVITIES

In the "Assigned" column below, put a check mark by each activity assigned to you by PLM, then proceed through your assigned activities. Check off each activity as you complete it. You may choose to do all of these activities or do some activities more than once.

<u>Assigned</u>	<u>Completed</u>	<u>Activity</u>	<u>Description</u>	<u>Page</u>
_____	_____	5-A	Reference Reading: Theory of Operation, Boolean Instructions 10 and 14; DPD ISC 3.2 Boolean Sequence. This learning activity covers the theory of operation for the 10 and 14 Boolean instructions.	5-5

CYBER 170 Model 720/730 CPU
Module 5

<u>Assigned</u>	<u>Completed</u>	<u>Activity</u>	<u>Description</u>	<u>Page</u>
_____	_____	5-B	Exercise: Theory of Operation Review, Boolean Instruction 10 and 14, DPD ISC 3.2 Boolean Sequence. This learning activity reinforces what you learned about the 10 and 14 Boolean instructions.	5-6
_____	_____	5-C	Reference Reading: Theory of Operation, Boolean Instructions 11, 12, 13 and 15, 16, 17, DPD ISC 3.2 Boolean Sequence. This learning activity covers the theory of operation for the 11, 12, 13 and 15, 16, 17 Boolean instructions.	5-9
_____	_____	5-D	Exercise: Theory of Operation Review, Boolean Instructions 11, 12, 13 and 15, 16, 17, DPD ISC 3.2 Boolean Sequence. This learning activity reinforces what you learned about the 11, 12, 13 and 15, 16, 17 Boolean instructions.	5-10
_____	_____	5-E	Reference Reading: Theory of Operation, Increment Instructions 50-57, DPD ISC 3.7 Increment Sequence. This learning activity covers the theory of operation for the 50-57 increment instructions.	5-13
_____	_____	5-F	Exercise: Theory of Operation Review, Increment Instructions 50-57, DPD ISC 3.7 Increment Sequence. This learning activity reinforces what you learned about the 50-57 increment instructions.	5-14

<u>Assigned</u>	<u>Completed</u>	<u>Activity</u>	<u>Description</u>	<u>Page</u>
_____	_____	5-G	Reference Reading: Theory of Operation, Increment Instructions 60-67, DPD ISC 3.7 Increment Sequence. This activity covers the theory of operation for the 60-67 increment instructions.	5-17
_____	_____	5-H	Exercise: Theory of Operation Review, Increment Instructions 60-67, DPD ISC 3.7 Increment Sequence. This learning activity reinforces what you learned about the 60-67 increment instructions.	5-18
_____	_____	5-I	Reference Reading: Theory of Operation, Increment Instructions 70-77, DPD ISC 3.7 Increment Sequence. This activity covers the theory of operation for the 70-77 increment instructions.	5-21
_____	_____	5-J	Exercise: Theory of Operation Review, Increment Instructions 70-77, DPD ISC 3.7 Increment Sequence. This learning activity reinforces what you learned about the 70-77 increment instructions.	5-22
_____	_____	5-K	Reference Reading: Theory of Operation, Integer Sum and Integer Difference Instructions (36 and 37), DPD ISC 3.7 Increment Sequence. This learning activity covers the theory of operation for the 36 and 37 integer sum and integer difference instructions.	5-25

CYBER 170 Model 720/730 CPU
Module 5

<u>Assigned</u>	<u>Completed</u>	<u>Activity</u>	<u>Description</u>	<u>Page</u>
_____	_____	5-L	Exercise: Theory of Operation Review, Integer Sum and Integer Difference (36 and 37), DPD ISC 3.7 Increment Sequence. This learning activity reinforces what you learned about the 36 and 37 integer sum and integer difference instructions.	5-26

**LEARNING ACTIVITY 5-A. REFERENCE READING:
THEORY OF OPERATION, BOOLEAN INSTRUCTIONS 10 AND 14,
DPD ISC 3.2, BOOLEAN SEQUENCE**

In this activity you will learn about the control signals and data paths utilized in the 10 and 14 Boolean instructions.

OBJECTIVE

- You will be able to locate, identify and describe the control signals and data flow for the 10 and 14 Boolean instructions.

Directions: Locate the following detailed pak diagram (DPD), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Model 720, 730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPD ISC 3.2.
- Theory of operation description for the 10 and 14 Boolean instructions.
- Instruction flow sequence chart, Boolean instructions 10 and 14.

Review the 10 and 14 instructions in the Hardware Reference Manual, publication number 60456100, if necessary.

Read the theory of operation description for the 10 and 14 Boolean instructions while referencing to DPD 3.2 and to the instruction flow sequence chart for the Boolean 10 and 14 instructions. Reference will also be necessary to various other DPDs in order to follow the control signal and data flow. DPDs will include IEC 3.1, 3.2, 3.6, and 3.7; ISC 3.2.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data flow for the 10 and 14 Boolean instructions, proceed to learning activity 5-B.

In learning activity 5-B you will answer questions designed to reinforce your ability to comprehend the logic associated with 10 and 14 Boolean instructions.

CYBER 170 Model 720/730 CPU
Learning Activity 5-B

LEARNING ACTIVITY 5-B. EXERCISE:
THEORY OF OPERATION REVIEW, BOOLEAN INSTRUCTIONS 10 AND 14,
DPD ISC 3.2 BOOLEAN SEQUENCE

This activity reinforces what you learned about the 10 and 14 Boolean instructions in learning activity 5-A.

OBJECTIVE

- You will be able to locate, identify and describe the control signals and data flow for the 10 and 14 Boolean instructions.

Directions: The following questions refer to the DPD, ISC 3.2, instruction flow sequence chart for 10 and 14 Boolean instructions and the theory of operation for the 10 and 14 Boolean instructions found in the CYBER 170 Model 720, 730 CPU Hardware Maintenance Manual, publication number 60456170.

Answer the questions by writing the most appropriate word or words in each blank. Compare your answers with those given at the end of this learning activity. Reread the theory of operation and analyze DPD 3.2 and the sequence flow chart (figure A-24) for any questions that were incorrectly answered.

1. Explain the operation performed by the 10 instruction.
XJ → XI
2. Explain the operation performed by the 14 instruction.
XK → XI
3. What is the module type and location for the Boolean sequence timing chain? GY-731
4. At what time is the Boolean exit signal (BOEXIT) issued?
T114
5. Define the data path for the 14 instruction starting with the X register.
XK → IS-C-RK1 → XI

6. On what DPD is each of the following located?
- a. X registers FECF, 2
 - b. I5 AU 3.5
 - c. C register AU 2.2
 - d. RK1 register AU 3.5
7. How many C Register bits are associated with each FC module? 3
8. Which FC module would be associated with bit 0 input to I5 coming from the x register? FC R 4.2
9. What module type is associated with the X register?
Y 2
10. What timing signal enables the transfer into X_i ?
CONT 4

CYBER 170 Model 720/730 CPU
Learning Activity 5-B

ANSWERS FOR LEARNING ACTIVITY 5-B

1. The quantity in X_j is transmitted to X_i .
2. The complement of the quantity in X_6 is transmitted to X_i .
3. GY module @ I31.
4. T114 of the Boolean sequence
5.
$$X_j \xrightarrow{\quad} I5 \xrightarrow{\quad} C \xrightarrow{\quad} RK1 \xrightarrow{\quad} X_i$$

$\begin{matrix} \text{IS2 0-47} \\ \text{C96-107} \end{matrix} \rightarrow \bar{X}_i$
6.
 - a. IEC 3.2
 - b. AU 3.3
 - c. AU 3.3
 - d. AU 3.5
7. Three
8. FC @ E26
9. UZ
10. COMX14 (COMT14)

**LEARNING ACTIVITY 5-C. REFERENCE READING:
THEORY OF OPERATION, BOOLEAN INSTRUCTIONS 11, 12, 13, AND 15, 16, 17
DPD ISC 3.2 BOOLEAN SEQUENCE**

In this activity you will learn about the control signals and data paths utilized in the 11, 12, 13 and 15, 16, 17 Boolean instructions.

OBJECTIVE

- You will be able to locate, identify and describe the control signals and data flow for the 11, 12, 13 and 15, 16, 17 Boolean instructions.

Directions: Locate the following detailed pak diagram (DPD), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Model 720, 730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPD ISC 3.2.
- Theory of operation for the 11, 12, 13 and 15, 16, 17 Boolean Instructions.
- Instruction flow sequence chart for Boolean instructions 11, 12, 13.
- Instruction flow sequence chart for Boolean instructions 15, 16, 17.

Review the description of the 11, 12, 13, 15, 16, and 17 instructions in the Hardware Reference Manual, publication number 60456100.

Review the 11, 12, 13 and 15, 16, 17 instructions in the Hardware Reference Manual, publication number 60456100.

Read the theory of operation description for the 11, 12, 13, 15, 16, and 17 instructions while referring to DPD ISC 3.2 and to the instruction flow sequence charts for the 11, 12, 13 and 15, 16, 17 instructions.

When you feel comfortable with your ability to locate, identify and describe the control signals and data flow for the 11, 12, 13 and 15, 16, 17 Boolean instructions, proceed to learning activity 5-D. In learning activity 5-D you will answer questions designed to reinforce your ability to comprehend the logic associated with the 11, 12, 13 and 15, 16, 17 Boolean instructions.

CYBER 170 Model 720/730 CPU
Learning Activity 5-D

LEARNING ACTIVITY 5-D. EXERCISE:

**THEORY OF OPERATION, BOOLEAN INSTRUCTIONS 11, 12, 13 AND 15, 16, 17
DPD ISC 3.2 BOOLEAN SEQUENCE**

This activity reinforces what you learned about the 11, 12, 13 15, 16 and 17 Boolean instructions in learning activity 5-C.

OBJECTIVE

- You will be able to locate, identify, and describe the control signals and data flow for the 11, 12, 13 and 15, 16, 17 Boolean instructions.

Directions: The following questions refer to the DPD, ISC 3.2, instruction flow sequence chart for 11, 12, 13, 15, 16 and 17 Boolean instructions and the theory of operation for the 11, 12, 13, 15, 16 and 17 Boolean instructions found in the CYBER 170 Model 720, 730 CPU Hardware Maintenance Manual, publication number 60456170.

Answer the questions by writing the most appropriate word or words in each blank. Compare your answers to those given at the end of this learning activity. Reread the theory of operation and analyze DPD 3.2 and the sequence flow chart (figure A-25, A-26) for any questions that were incorrectly answered.

1. What is the logical operation performed by the 11 instruction? LOGICAL Product $X_j \cdot X_k \rightarrow X_l$
2. What is the logical operation performed by the 12 instruction? Logical sum
3. What is the logical operation performed by the 13 instruction? Logical Difference
4. When does the X_j contents enter the C Register? T50 Ground level
5. What signal enables transfer of X_j contents to bits 48-107 of the I5 Selector? NB114
6. What signal suppresses the end around carry function of the D Adder during logical operations? N2114
7. What are the differences between 11, 12 and 13 instructions compared to 15, 16 and 17 instructions? X_k is complemented
8. How is the X_k compliment accomplished? normal I5
out is not blocked
BL15C not up from 13, 15, 17

CYBER 170 Model 720/730 CPU
Learning Activity 5-C

The answers to this learning activity are on the following page.

10-11

CYBER 170 Model 720/730 CPU
Learning Activity 5-D

ANSWERS FOR LEARNING ACTIVITY 5-D

1. Logical product (AND)
2. Logical series (OR)
3. Logical difference (exclusive OR)
4. Initial common time
5. NB 114
6. Ni 114
7. X_k is complemented
8. BL15C does not occur, so X_k from the I5 selector remains complemented.

**LEARNING ACTIVITY 5-E. REFERENCE READING:
THEORY OF OPERATION, INCREMENT INSTRUCTIONS 50-57
DPD ISC 3.7 INCREMENT SEQUENCE**

In this activity you will learn about the control signals and the data paths utilized in the 50-57 increment instructions.

OBJECTIVE

- You will be able to locate, identify and describe the central signals and data flow for the 50-57 increment instructions.

Directions: Locate the following detailed pak diagram (DPD), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Model 720, 730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPD ISC 3.7.
- Theory of operation for the 50-57 increment instructions.
- Instruction flow sequence chart for increment instructions 50-57.

Review the 50-57 instructions in the Hardware Maintenance Manual, publication number 60456100.

Read the theory of operation description for the 50-57 increment instructions while referring to DPD ISC 3.7 and to the instruction flow sequence chart for the 50-57 increment instructions.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data flow for the 50-57 increment instructions, proceed to learning activity 5-F. In learning activity 5-F you will answer questions designed to reinforce your ability to comprehend the logic associated with the 50-57 increment instructions.

CYBER 170 Model 720/730 CPU
Learning Activity 5-F

LEARNING ACTIVITY 5-F. EXERCISE:
THEORY OF OPERATION, INCREMENT INSTRUCTIONS 50-57
DPD ISC 3.7 INCREMENT SEQUENCE REVIEW

This activity reinforces what you learned about the 50-57 increment instructions in learning activity 5-E.

OBJECTIVE

- You will be able to locate, identify and describe the control signals and data flow for the 50-57 increment instructions.

Directions: The following questions refer to the DPD, ISC 3.7, instruction flow sequence chart for 50-57 increment instructions and the theory of operation for the 50-57 increment instructions found in the CYBER 170 Model 720, 730 CPU Hardware Maintenance Manual, publication number 60456170.

Answer the questions by writing the most appropriate word or words in each blank and then compare the answers to the correct answers at the end of this learning activity. Reread the theory of operation and analyze DPD ISC 3.7 and the sequence flow chart (figure A-14, A-15) for any questions that were incorrectly answered.

1. What is the module type and location for the module containing the increment sequence timing chain?
VA-H31
2. What is the logical operation performed by the 50 instruction? SET AI TO AI+K
3. What use is made of the result stored in the Ai register?
from address, to get data into X-301
from X6 X7 data from register
4. Where does the first operand come from in the 52 instruction? XJ
5. How many bits are sent to the E register during a 52 instruction? 18
6. What registers are used as an input to the F adder?
F

CYBER 170 Model 720/730 CPU
Learning Activity 5-F

7. What happens when an address out of range is detected and the i value is 6? $X_i = \text{original contents of memory in body of}$ Address unchanged
8. What happens when an address out of range is detected on i=5? $X_i = 05$ Address unchanged
9. What is the unique about the selection of K as in the 50, 51 and 52 instructions? PC count is incremented
10. Where is the second operand in the 50 instructions obtained? K

CYBER 170 Model 720/730 CPU
Learning Activity 5-F

ANSWERS FOR LEARNING ACTIVITY 5-F

1. YA @ H31
2. One's complement addition or subtraction of 18-bit operands.
3. The result started in Ai is used as the CM relative address, then the CPU reads or writes to that address.
4. Xj
5. 18
6. E and F registers
7. Xi retains its original contents and the contents of Ai are unchanged.
8. Xi is loaded with all zeros and the contents of memory location Ai are unchanged.
9. The selection of K advances the parcel counter for selection of the next instruction since K is part of the instruction being executed and would otherwise be selected as an instruction.
10. The K portion of the instruction.

**LEARNING ACTIVITY 5-G. REFERENCE READING:
THEORY OF OPERATION, INCREMENT INSTRUCTIONS 60-67
DPD ISC 3.7 INCREMENT SEQUENCE**

In this activity you will learn about the control signals and the data paths utilized in the 60-67 increment instructions.

OBJECTIVE

- You will be able to locate, identify and describe the control signals and data flow for the 60-67 increment instructions.

Directions: Locate the following detailed pak diagram (DPD), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Model 720, 730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPD ISC 3.7.
- Theory of operation for the 60-67 increment instructions.
- Instruction flow sequence chart for increment instructions 60-67.

Review the 60-67 instructions in the Hardware Maintenance Manual, publication number 60456100.

Read the theory of operation description for the 60-67 increment instructions while referring to DPD ISC 3.7 and to the instruction flow sequence chart for the 60-67 increment instructions.

When you feel comfortable with your ability to locate, identify and describe the control signals and data flow for the 60-67 increment instructions, proceed to learning activity 5-H. In learning activity 5-H you will answer questions designed to reinforce your ability to comprehend the logic associated with the 60-67 increment instructions.

CYBER 170 Model 720/730 CPU
Learning Activity 5-H

LEARNING ACTIVITY 5-H. EXERCISE:
THEORY OF OPERATION, INCREMENT INSTRUCTIONS 60-67
DPD ISC 3.7 INCREMENT SEQUENCE REVIEW

This activity reinforces what you learned about the 60-67 increment instructions in learning activity 5-G.

OBJECTIVE

- You will be able to locate, identify and describe the control signals and data flow for the 60-67 increment instructions.

Directions: The following questions refer to the DPD ISC 3.7 instruction flow sequence chart for the 60-67 increment instructions, and the theory of operation for the 60-67 increment instructions found in the CYBER 170 Model 720, 730 CPU Hardware Maintenance Manual, publication number 60456170.

Answer the following questions by writing the most appropriate word or words in each blank. Compare your answers to those given at the end of this activity. Reread the theory of operation and analyze DPD ISC 3.7 and the sequence flow chart (figure A-16) for any questions that were incorrectly answered.

1. What function is performed by the 60 instruction?
 $B_j = (A_j) + K$
2. What function is performed by the 67 instruction?
 $B_j = (B_j) - (R/K)$
3. At what time is the A_j , B_j or X_j passed to the I3 selector and to the E register? Common Turn
4. What signal enables the F register to receive the B_k or K from the I3 selector at T114? NI114
5. What signal enables the complimenting the output of the I3 selector at T114 fo the 65 and 67 instructions? NI114A

CYBER 170 Model 720/730 CPU
Learning Activity 5-H

The answers to this learning activity are on the following page.

CYBER 170 Model 720/730 CPU
Learning Activity 5-H

ANSWERS FOR LEARNING ACTIVITY 5-H

1. Set B_i to $A_j + K$
2. Set B_i to $B_j - K$
3. common time
4. Ni 114
5. In 114a

**LEARNING ACTIVITY 5-I. REFERENCE READING:
THEORY OF OPERATION, INCREMENT INSTRUCTION 70-77
DPD ISC 3.7 INCREMENT SEQUENCE**

In this activity you will learn about the control signals and the data paths utilized in the 70-77 increment instructions.

OBJECTIVE

- You will be able to locate, identify and describe the control signals and data flow for the 70-77 increment instructions.

Directions: Locate the following detailed pak diagram (DPD), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Model 720, 730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPD ISC 3.7.
- Theory of operation for the 70-77 increment instructions.
- Instruction flow sequence chart for increment instructions 70-77.

Review the 70-77 instructions in the Hardware Maintenance Manual, publication number 60456100.

Read the theory of operation description for the 70-77 increment instructions while referring to DPD ISC 3.7 and to the instruction flow sequence chart for the 70-77 increment instructions.

When you feel comfortable with your ability to locate, identify and describe the control signals and data flow for the 70-77 increment instructions, proceed to learning activity 5-J. In learning activity 5-J you will answer questions designed to reinforce your ability to comprehend the logic associated with the 70-77 increment instructions.

CYBER 170 Model 720/730 CPU
Learning Activity 5-J

LEARNING ACTIVITY 5-J. EXERCISE:
THEORY OF OPERATION, INCREMENT INSTRUCTION 70-77
DPD ISC 3.7 INCREMENT SEQUENCE

This activity reinforces what you learned about the 70-77 increment instructions in learning activity 5-I.

OBJECTIVE

- You will be able to locate, identify and describe the control signals and data flow for the 70-77 increment instructions.

Directions: The following questions refer to the DPD ISC 3.7 instruction flow sequence chart for the 70-77 increment instructions, and the theory of operation for the 70-77 increment instructions found in the CYBER 170 Model 720, 730 CPU Hardware Maintenance Manual, publication number 60456170.

Answer the questions by writing the most appropriate word or words in each blank. Compare your answers to those given at the end of this activity. Reread the theory of operation and analyze DPD ISC 3.7 and the sequence flow chart (Figure A-17) for any questions that were incorrectly answered.

1. What function is performed by the 72 instruction?
 $X_j = (X_j) + K$
2. What function is performed by the 76 instruction?
 $X_j = (B_j) / (RK)$
3. Where are results stored for 7X instructions?
~~X~~
4. How is the sign of the result handled when storing an 18 bit result in a 60-bit register? SIGN EXTENDED
5. What signal enables the exit from the increment instruction at T214? N/NEXB

CYBER 170 Model 720/730 CPU
Learning Activity 5-J

The answers to this learning activity are on the following page.

CYBER 170 Model 720/730 CPU
Learning Activity 5-J

ANSWERS FOR LEARNING ACTIVITY 5-J

1. Set X_i to $X_j + K$
2. Set X_i to $B_j + B_k$
3. Lower 18 bits of the X_i register
4. The sign is extended into the upper 42 bits of X_i
5. Ninexa

**LEARNING ACTIVITY 5-K. REFERENCE READING:
THEORY OF OPERATION, INTEGER SUM AND INTEGER
DIFFERENCE INSTRUCTIONS 36, 37, DPD ISC 3.7
INCREMENT SEQUENCE**

In this activity you will learn about the control signals and the data paths utilized in the 36 and 37 integer sum and integer difference instructions.

OBJECTIVE

- You will be able to locate, identify and describe the control signals and data flow for the 36 and 37 integer sum and integer difference instructions.

Directions: Locate the following detailed pak diagram (DPD), theory of operation description, and the instruction flow sequence chart found in the CYBER 170 Model 720, 730 CPU Hardware Maintenance Manual, publication number 60456170:

- DPD ISC 3.7.
- Theory of operation for the 36 and 37 integer sum and difference instructions.
- Instruction flow sequence chart for the 36 and 37 integer sum and difference instructions.

Review the 36 and 37 instructions in the Hardware Maintenance Manual, publication number 60456100.

Read the theory of operation description for the 36 and 37 integer sum and difference instructions while referring to DPD ISC 3.7 and to the instruction flow sequence chart for the 36 and 37 increment instructions.

When you feel comfortable with your ability to locate, identify, and describe the control signals and data flow for the 36 and 37 integer sum and difference instructions, proceed to learning activity 5-L. In learning activity 5-L you will answer questions designed to reinforce your ability to comprehend the logic associated with the 36 and 37 integer sum and difference instructions.

LEARNING ACTIVITY 5-L. EXERCISE:
THEORY OF OPERATION INTEGER SUM AND INTEGER DIFFERENCE 36, 37
DPD ISC 3.7 INCREMENT SEQUENCE

This activity reinforces what you learned about the 36 and 37 integer sum and difference instructions in learning activity 5-E.

OBJECTIVE

- You will be able to locate, identify and describe the control signals and data flow for the 36 and 37 integer sum and difference instructions.

Directions: The following questions refer to the DPD, ISC 3.7, instruction flow sequence chart for 36 and 37 integer sum and difference instructions and the theory of operation for the 36 and 37 integer sum and difference instructions found in the CYBER 170 Model 720, 730 CPU Hardware Maintenance Manual, publication number 60456170.

Answer the questions by writing the most appropriate word or words in each blank. Compare them to the answers with those given at the end of this learning activity. Reread the theory of operation and analyze DPD ISC 3.7 and the sequence flow chart (figure A-13) for any questions that were incorrectly answered.

1. What is the function of the 36 instruction? _____
 $X_i = X_j + X_k$
2. What is the function of the 37 instruction? _____
 $X_i = X_j - X_k$
3. Which adder is used to perform the register addition?
D adder
4. What path is followed for entering the X_j information into the C register? $X_j \rightarrow I5 \rightarrow C$
5. What signal enables the D register at T114 to receive the X_j operand from the I4 selector? INX 14

CYBER 170 Model 720/730 CPU
Learning Activity 5-L

The answers to this learning activity are on the following page.

CYBER 170 Model 720/730 CPU
Learning Activity 5-L

ANSWERS FOR LEARNING ACTIVITY 5-L

1. Integer sum of X_j and X_k to X_i
2. Integer difference of X_j and X_k to X_i
3. D adder
4. X_j I5 Selector C
5. Inx14

POST TEST

When you have completed the learning activities assigned for module 5, sign on to the PLATO terminal and take the module 5 test.

Depending on the results of the test, you will be told to either review some of the previous activities, or to go on to module 6.

COMMENT SHEET

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PUBLICATION NO. 75445734 REVISION A Prod. No. R0404

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